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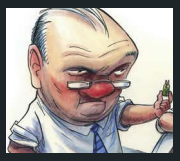

HANDCRAFTED ANALOG GETS AUTOMATED ASSIST

Page 40

SHEDDING LIGHT ON **EMBEDDED DEBUGGING**

Page 29

USING FPGAs IN CONSUMER ELECTRONICS

Page 49

OPTIMIZE MEMORY-SYSTEM DESIGN FOR MULTIMEDIA APPLICATIONS

Page 59

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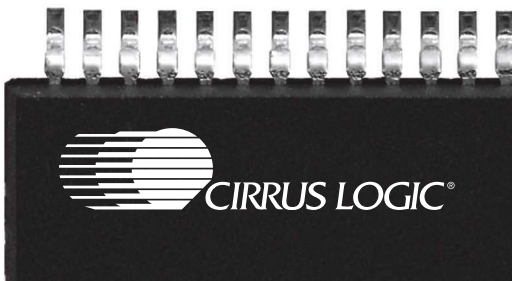

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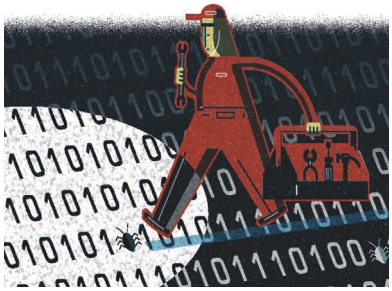
by Rick Nelson, Editor-in-Chief



Shedding light on embedded debugging

by Robert Cravotta, Technical Editor

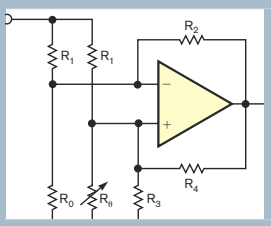
Using FPGAs in consumer electronics

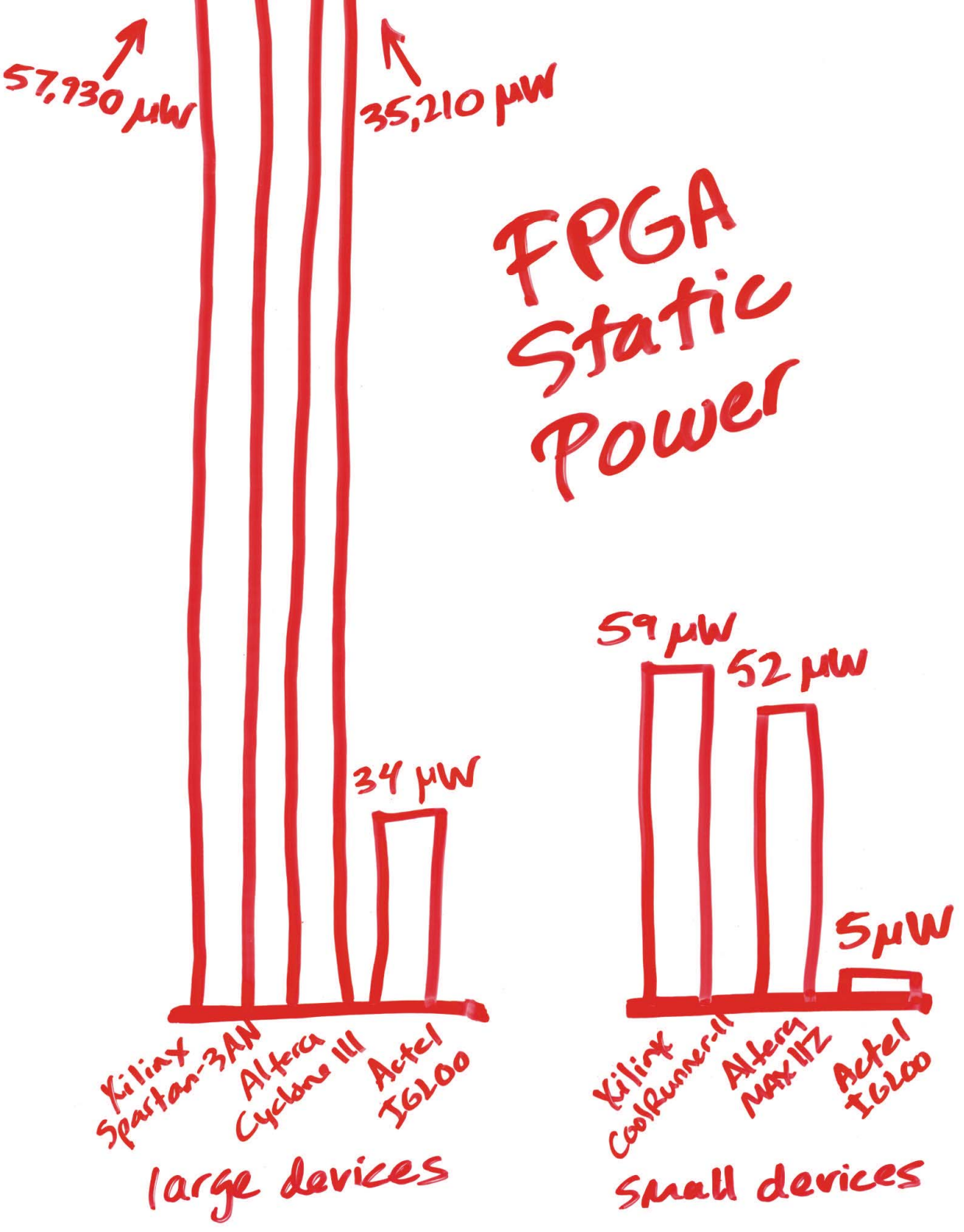
by Phuttachad Thiencharoenwong, SingMai Electronics

Optimize memory-system design for multimedia applications

by David Lautzenheiser and Agha Hussain, Silistix

DESIGNIDEAS





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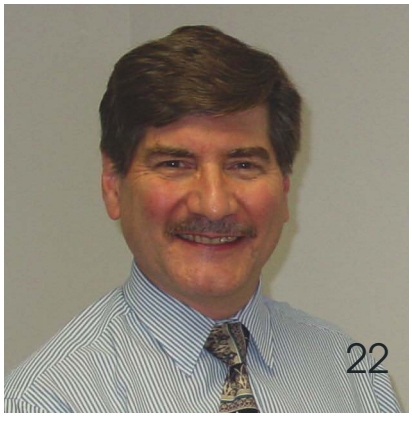
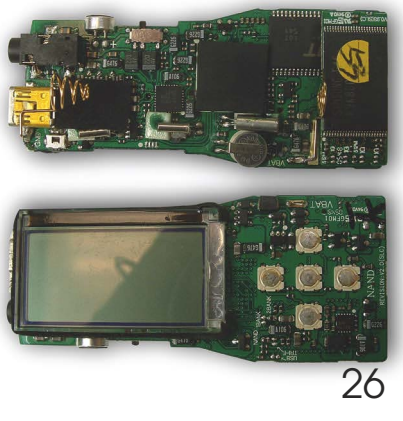
contents 9.4.08

pulse

Dilbert 16



22



26

83

DEPARTMENTS & COLUMNS

PRODUCT ROUNDUP

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THIS WEEK IN GEEK

EDN's Friday tech roundup, available in the *Now Hear This* blog.
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BY RON WILSON, EXECUTIVE EDITOR

Oil prices, technology, and the cost of ignorance

The world has just had a graphic demonstration of the workings of supply and demand in the oil industry. Supply of sweet, light crude became insufficient for the demand, and its price shot up. In response to the higher prices, demand for gasoline in the United States dropped, and the price shot back down again. In light of this dramatic performance, it is worth asking whether quick, technically feasible applications of electronics could significantly reduce demand in the short term.

We are looking for feasible and fast solutions, so converting the entire Western world's vehicle fleet to fuel cells is out. So is covering two Southwestern states with photovoltaic cells or building a set of experimental but full-scale fusion reactors. Relatively quick measures do exist, however, and, unsurprisingly, they focus not on fundamental changes in society but on increasing efficiency.

One example dear to the hearts of many commuters is traffic control. In much of North America and, from the little we have seen, industrializing Asia, the entire notion that you can enhance rather than impede the flow of traffic by properly regulating traffic lights is an as-yet-unmade discovery. The cost of this ignorance is horrendous. Estimates show that a third of the fuels vehicles in urban areas consume go to waste because of unnecessary acceleration, almost entirely after a traffic control or jam has slowed the vehicle. Technologically simple computerized sensor and control networks and known algorithms could cut this waste by a large factor. The amount of necessary capital equipment and labor would be trivial in comparison with the savings and within the resources of even state-level governments without huge national subsidies. The only shortage is in the skill to install and operate the networks and the knowledge to recognize the problem.

Estimates show that a third of the fuels vehicles in urban areas consume go to waste because of unnecessary acceleration.

Public transportation presents a similar example. Most municipalities in the world wear about their necks as a token of honor an ever-moving, constantly belching necklace of huge diesel buses, with a ratio of average payload weight to vehicle weight that would embarrass a Hummer owner. Municipalities could inexpensively replace most of these monstrosities with fuel-efficient small vans, directed by a network of GPS (global-position-system) sensors, traffic monitors, requester terminals, and computers, creating an on-demand public-transit network that would function at a fraction of the fuel consumption and congestion generation of the behemoths. Again, there is no new technology here, and adequately suitable vehicles are currently languishing in automotive-dealer inventories.

Or consider where the demand for all that sweet, light crude oil comes from. The most dramatic increase isn't from sport-utility vehicles or corporate jets. It's from diesel generators because, in much of the developing world, local demand for electricity—partly created by our desire for cell phones and TV sets—is soaring. In countries that lack generation and distribution infrastructure, only local diesel generators can meet that demand. Hence, the demand for diesel soars—driving refineries to capacity and creating a shortage of sweet, light crude oil. (There is no shortage or price premium for high-sulfur crude, by the way. Few refineries can produce diesel from it.) So what would be the impact on demand if we focused our photovoltaic and storage efforts and subsidies not on wealthy North Americans' rooftops, but on developing-world towns and villages?

Many such opportunities exist to use a little understanding, a little technology, and a little capital to make a significant decrease in fuel consumption. And, as noted, a small decrease in consumption can make a big difference in global inflation pressure. But rest assured that these things will not happen. Inefficiency is one of the costs nature imposes as the price of public ignorance of technology. EDN

Contact me at ronald.wilson@reedbusiness.com.

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More Q. Less Cu

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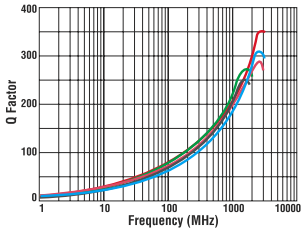
63.546

These tiny new air core inductors have the highest Q and current handling in the smallest footprint.

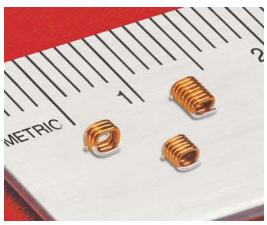
Coilcraft's new SQ air core inductors have unmatched Q factors: most are above 200 in the 1-2 GHz range! That's 3 times higher than comparably sized 0805 chip coils.



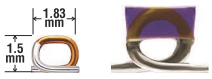
Q factors are 3X higher than standard chip inductors

And with their extremely low DCR, they can handle 4 to 8 times more current: up to 4.4 Arms.

SQ air core inductors are perfect for your LC filter and RF impedance matching applications. They come in 15 values ranging from 6 to 27.3 nH, all with 5% tolerance.



These coils are significantly smaller than existing air core inductors. We reduced the footprint by using close-wound construction and keeping the leads close to the body. The square shape cuts the height to as low as 1.5 mm and creates flat top and bottom surfaces for easy automated handling and stable mounting.



The square shape and narrow footprint reduce board space by 60-75% over conventional air core inductors.

See how the ultra-high Q and current handling of Coilcraft's new SQ air core inductors can maximize the performance of your next design. For complete specifications and free evaluation samples, visit **www.coilcraft.com/sq**

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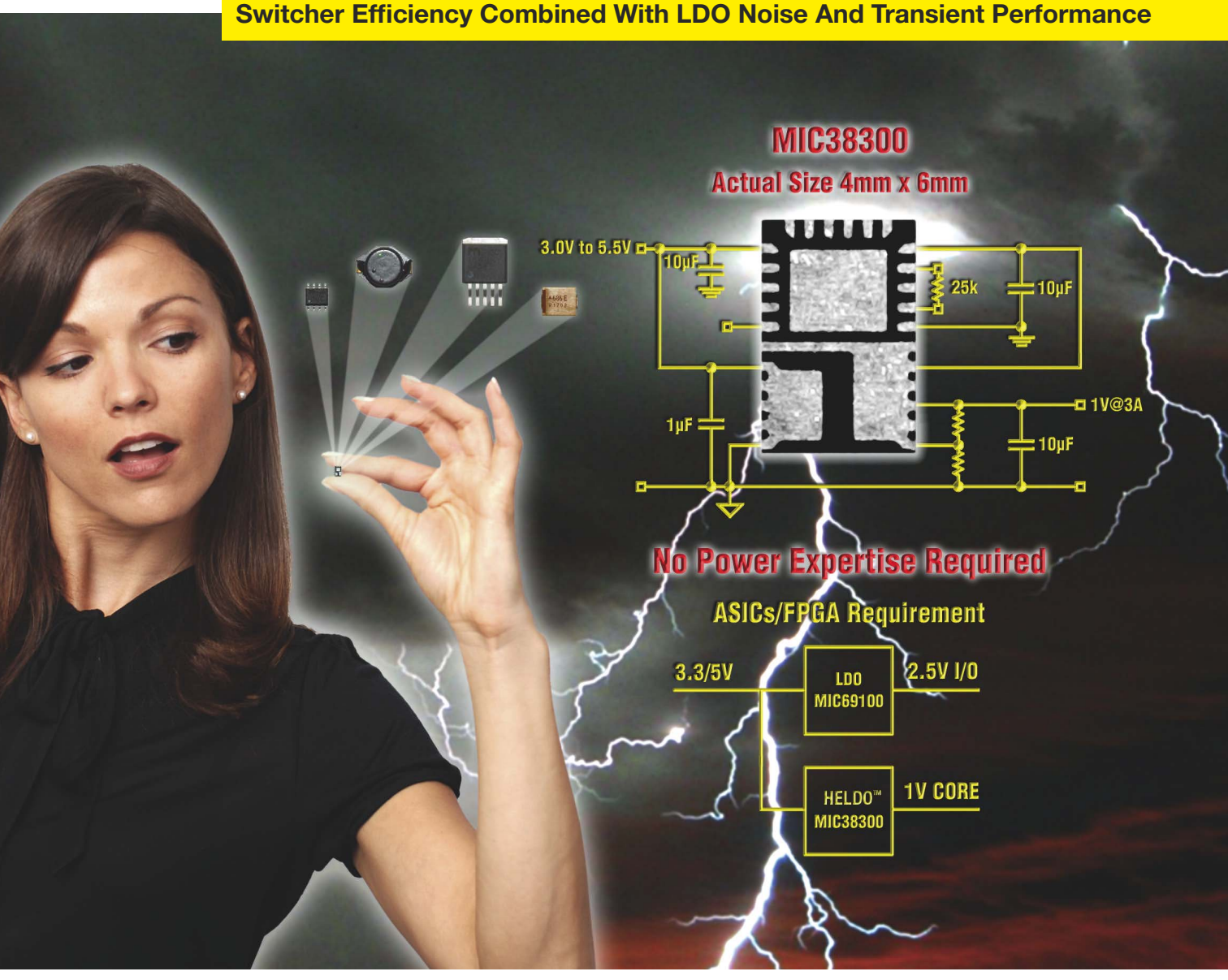

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$P_{ff} =$

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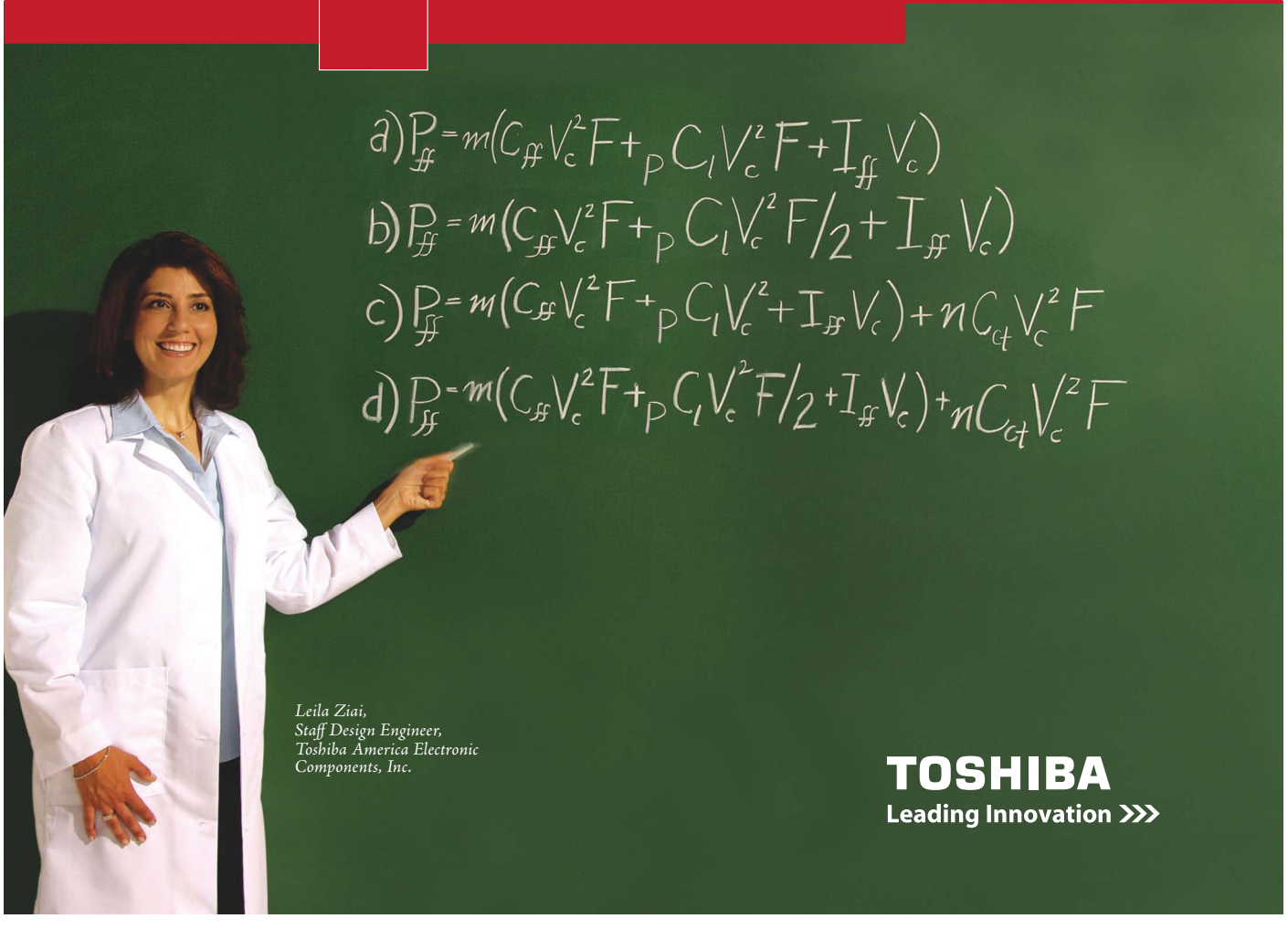

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Staff Design Engineer,
Toshiba America Electronic Components, Inc.

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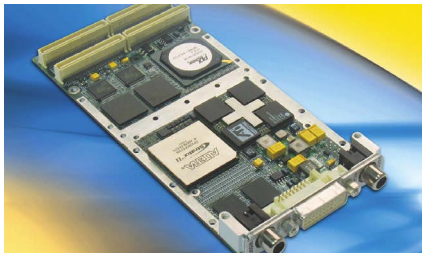
INNOVATIONS & INNOVATORS

Video, graphics module drives dual displays

With advanced-sensor-fusion, image-manipulation, and tactical-moving-map applications in mind, Aitech Defense Systems recently introduced the M590 graphics and video PMC (peripheral-component-interconnect-mezzanine-card) module that simultaneously outputs information from two independent data streams to two analog or digital displays. The new M590 supports 2- or 3-D-video displays plus image capture with overlay and underlay features to provide man-machine interfaces with resolutions as high as 1536×2048 pixels at 30- to 200-Hz refresh rates and as many as 32 bits per pixel.

An AMD ATI (www.amd.com) M9 graphics processor with an on-chip 64-Mbyte frame-buffer array and dual RAMDAC (random-access-memory-digital-to-analog-converter) units power the M590, which performs high-speed 2-D-line, 3-D-polygon, and texture acceleration. The module also supports multiple video-input and -output formats, including NTSC (National Television System Committee) and PAL (phase-alternating line) for both interlaced and noninterlaced monitors. For advanced video-display applications,



Aitech's new PMC drives dual 2- or 3-D-video displays from independent data streams at resolutions as high as 1536×2048 pixels.

the M590 provides video overlay and underlay functions that generate images, superimpose an input from one of the various video formats, and drive the result to a monitor. The module's software package supports all onboard capabilities and features OpenGL drivers for both VxWorks and Integrity real-time operating systems. The M590 is available in commercial-, rugged-, and military-temperature ranges and in either conduction- or air-cooled versions. The price for an M590 starts at $3440 (OEM quantities).**—by Warren Webb**

▷**Aitech Defense Systems Inc**, www.rugged.com.

FEEDBACK LOOP

"A young graduate I once worked with told me he got into engineering for one reason—to learn a bit about engineering so that he could go back to school to get a law degree and get rich by suing big corporations over engineering patents."

—Reader and frequent *EDN* contributor Glen Chenier, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6578140. Add your comments.

AMD updates Stream software-development kit

To help increase the ease and efficiency of software development using its Stream-processing approach, microprocessor challenger AMD (Advanced Micro Devices) recently announced an extensive set of upgrades for future versions of the Stream software-development kit. AMD intends that these upgrades will reduce the time and effort required to produce GPU (graphics-processing-unit)-accelerated applications that run on multiple platforms, with expanding support for industry-standard APIs (application-programming interfaces) and enhanced support for C/C++. The updates will add full support for DirectX 11, the next-generation suite of advanced APIs from Microsoft (www.microsoft.com).

DirectX 11 builds on the performance of DirectX 10.1 for 3-D-graphics rendering and gaming control and includes new technologies to ease the creation of general-purpose graphics-processing-accelerated applications that can run on any Windows Vista-powered platform. AMD is supporting efforts to develop OpenCL as an open standard and plans to evolve the Stream software-development kit to comply with OpenCL. The company is continuing to give developers the option of creating and using their own programming languages and high-level tools.

—by Ann Steffora Mutschler

▷**Advanced Micro Devices Inc**, www.amd.com.

Touch-panel controller targets media-device interfaces

Atmel, in the form of its recently acquired subsidiary, Quantum Research Group, has introduced a touch controller that combines a slider control with buttons, an integrated LED controller, and GPIO (general-purpose-input/output) functions. The AT42QT2160, part of the company's new QTouch series, uses charge-transfer technology to control as many as 16 touch keys with a slider that you can configure to use two to eight of the touch-key channels. If you need an extra-long slider control, you can add interpolation between points with a resistive-touch-sensor element.

The chip can also control as many as 11 LEDs through a host-controlled PWM-output function, eliminating the need for an external LED controller.

Atmel designed the device for use as a multimedia-HMI (human-machine-interface) controller in mobile phones and consumer electronics, such as personal media players. It operates from 1.8 to 5.5V, and you can also use it in applications such as digital still cameras, PDAs (personal digital assistants), and handheld gaming devices. Like previous chips using the charge-transfer technology, the 2160 claims high immunity to EMI (electromagnetic interference) through spread-spectrum modulation and filtering algorithms, calibration of the device over its lifetime, and designer-defined sensitivity thresholds for individual keys. AKS (adjacent-key suppression) intelligently suppresses signals from nearby keys so that only the keys that a user intends to touch register a touch.

> The 2160 claims high immunity to EMI.

The AT42QT2160 has three GPIOs with PWM capability and eight shared-output ports that provide additional standard outputs for the host without adding cost or using an extra I/O-expansion device. You configure the device with an I^2C (inter-integrated-circuit) interface. You might design touch-button-sensor electrodes of any arbitrary size greater than 6×6 mm and of arbitrary shape, as copper pads on the PCB (printed-circuit board) or a flexible circuit. The chip senses touches to those pads through glass or plastic as thick as 2.5 mm.

Samples of the AT42QT2160 are available now in a 28-pin, 4×4-mm QFN package; it sells for 98 cents (10,000). An evaluation board, which comes with an I^2C-to-USB converter to connect to a PC, costs $82.50.

—by Graham Prophet

▷**Atmel**, www.atmel.com.

Atmel's QTouch controller integrates enough functions to control a complete media device.

MODULE TARGETS EMBEDDED-SYSTEM DESIGN

09.04.08

Building on its popular FPGA-based PXI (PCI extensions for instrumentation), PC, and CompactRIO (reconfigurable-input/output) platforms, National Instruments has announced a new line of single-board RIO modules that offers a lower-cost, integrated-hardware option for embedded control and data-acquisition applications. The RIO-96xx devices combine a real-time embedded processor, a reconfigurable FPGA, and analog and digital I/O on an 8.2×5.6-in. PCB (printed-circuit board). Designers can use the company's LabView software to configure the RIO hardware and the application's embedded firmware.

The modules feature a 266- or 400-MHz Freescale (www.freescale.com) MPC5200 processor, the Wind River (www.windriver.com) VxWorks real-time operating system, and a Xilinx (www.xilinx.com) Spartan-3 FPGA. The onboard analog and digital I/O connects to the FPGA to provide low-level customization of timing- and I/O-signal processing. You can expand the I/O capabilities using three expansion slots for custom hardware or any C-Series I/O module. Prices for the devices start at $1000 (100 or more). Watch a demonstration video at www.ni.com/singleboard.

—by Warren Webb

▶**National Instruments, www.ni.com.**

DILBERT By Scott Adams

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Agilent Technologies

Power-supervision IC measures regulator-input current, differential-output voltage

Summit Microelectronics' new SMM151 power-supervision IC allows digital control and monitoring of any voltage regulator. The device monitors input current to the target regulator so there is no added impedance to the output rail. A differential pair that can accept 15V inputs performs the voltage sensing, which is accurate to ±1%; current-sensing accuracy is ±2%.

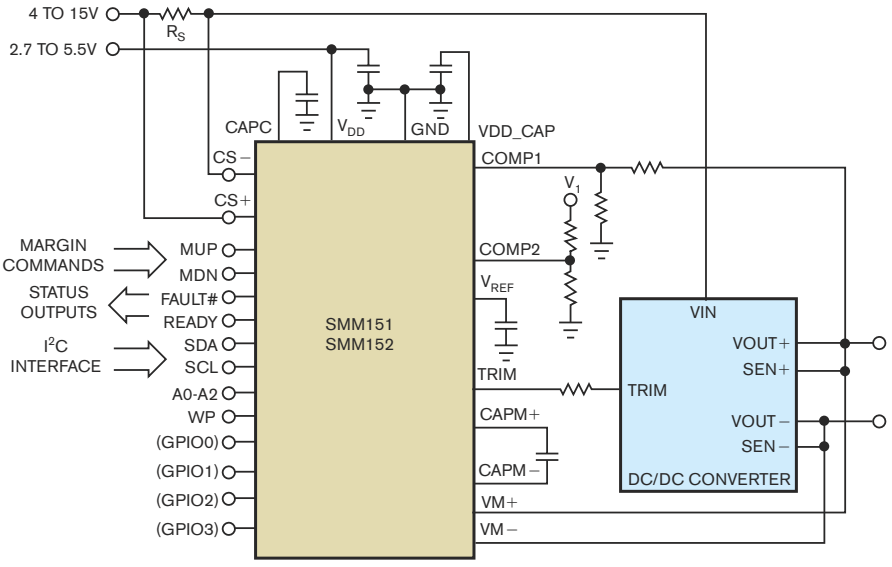
The part operates from 2.7 to 5.5V of power and has an I²C (inter-integrated-circuit) interface that allows system monitoring in real time with parameters that you can change using the I²C bus. The unit provides fault- and ready-status outputs and accepts margin commands on two dedicated pins or the I²C bus.

The IC allows users to program limits for glitch-filter duration, margin delays, and response to fault conditions. A sister part, the SMM152, also has four general-purpose I/O pins. Developers can program the power-on state of these pins and store that information in nonvolatile memory within the IC. All family members have two comparators for detecting levels or providing window comparisons, and they target applications in computing and datacom equipment, servers, wireless routers, and other high-reliability systems.

The SMM151EV evaluation board works through a USB port with Summit's Windows-based GUI (graphical user interface), which allows designers to set up the operating parameters and then program them into nonvolatile memory. Once designers define the device's functions, they can extract a hex file from the evaluation board that allows Summit to provide the part in volume quantities.

The device operates in a 0 to 70 or a −40 to +85°C temperature range and comes in a 5×5-mm, 28-pad QFN package. The SMM151 and SMM152 sell for $3.49 and $3.79 (1000), respectively. Samples and the SMM151EV evaluation modules are available, and volume production has begun.**—by Paul Rako**

▷**Summit Microelectronics**, www.summitmicro.com/SMM151.



The SMM151 power-supervisor IC provides voltage and current measurement as well as margining and supervisory functions.

EDNBLOG

EMBEDDED WEBBLOG

Beagle Board opens embedded development

OFFERING DESIGNERS and hobbyists a low-cost starting point for device development, Digi-Key, Texas Instruments, and a group of volunteers have joined forces to create an open, single-board-computer design that can be adapted to a multitude of embedded projects. The module, dubbed the Beagle Board, is a low-power, fanless design incorporating TI's recently introduced OMAP35x processors based on the ARM Cortex-A8 core.

The design reduces cost and power requirements by eliminating most onboard peripherals, except those provided by the processor, and incorporating standard expansion buses, like high-speed USB 2.0 and SDIO for application-specific I/O. The processor contains 2-D- and 3-D-graphics acceleration capabilities plus a DSP optimized for multimedia processing.

Further simplifying development, the board is completely powered by the onboard USB interface used for downloading the software from a laptop or desktop computer. The open-source-software-development community provides a Linux operating system specifically configured for the Beagle Board.

A 132-pg hardware-reference manual is available for download at the BeagleBoard.org Web site and provides complete module component descriptions, schematics, and board-manufacturing documentation.

—by Warren Webb

▶www.edn.com/webblog.

▶For the full post, go to www.edn.com/080904b1.

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In their quest for near-100% uptime, designers of high-availability-system applications, such as telecom and datacom servers, employ redundant-power systems: If one power supply fails, a redundant supply can pick up the load. Redundant- and backup-power supplies enter the load along with ORing MOSFETs, which ideally should have a minimal on-state resistance and fast dynamic response to power source failures.

Picor's Cool-ORing family, comprising the PI2121, PI2123, and PI2125 devices, integrates high-speed ORing-MOSFET controllers with low-on-state-resistance MOSFETs that typically achieve a dynamic response within 160 nsec. The 8V, 24A PI2121 targets use in applications with bus voltages of 5V or lower; the 15V, 15A PI2123 suits applications with bus voltages of 9.6V or lower; and the 30V, 12A PI2125 suits applications with bus voltages of 12V. The typical on-state resistances for the three parts are 1.5, 3, and 5.5 mΩ, respectively. Each part can also work in parallel to address higher current requirements through a master/slave feature. The devices detect normal-forward, excessive-forward, light-load, and reverse-current flow through their internal MOSFETs, and they report fault conditions through an active low-fault-flag output. A temperature-sensing function indicates a fault if the maximum junction temperature exceeds 160°C. You can program the undervoltage and overvoltage thresholds using external resistor dividers.

Picor's Cool-ORing family of devices integrates high-speed ORing-MOSFET controllers with low-on-state-resistance MOSFETs that achieve a typical dynamic response of 160 nsec and a typical on-state resistance as low as 1.5 mΩ.

The family also includes discrete versions of the ORing controllers. The high-speed, active-ORing PI2001 controller targets use with industry-standard single or paralleled MOSFETs; the PI2003 controller suits use in −48V, redundant-power architectures and systems requiring operation during input-voltage transients as high as 100V for 100 msec; and the high-speed, active-ORing P12002 controller IC has a load-disconnect feature that functions like that of the PI2122 but works with industry-standard, back-to-back N-channel MOSFETs.

The PI2121, PI2123, and PI2125 come in 17-pin, 5×7×2-mm-high, thermally enhanced LGA packages and sell for $1.98 (10,000). The discrete Cool-ORing controllers are available in 3×3-mm, 10-lead TDFN packages and sell for 84 cents for the PI2001 and PI2003 and 92 cents (10,000) for the PI2002. An eight-lead SOIC-package option costs 76 cents for the PI2001 and PI2003 and 83 cents for the PI2002 (10,000).

—by Margery Conner

▷**Picor**, www.vicorpower.com/picorpower.

EDN BLOG

BRIAN'S BRAIN

HDD (and SSD) capacities: up, up, and away

IT SEEMS LIKE just yesterday that I was first writing to you about the world's first 1-Tbyte, 3.5-in. HDD (hard-disk drive). Hitachi's accomplishment didn't remain sole-sourced long, of course, given the hypercompetitiveness of the HDD industry. Seagate launched a four-platter (250-Gbyte/platter) configuration in June 2007, along with a Samsung paper launch of a three-platter (333-Gbyte/platter) configuration in that same time frame. Western Digital waited until late July 2007 to unveil its own four-platter configuration, and recent data suggests that Samsung's products are finally shipping in volume (as well that 1-Tbyte drives have dipped below $150!).

Recent announcements show that vendors' competitive juices have by no means abated, even in the slightest. On July 9, Hitachi finally got its 1-Tbyte drive down to a three-platter configuration, the 7200-rpm Deskstar 7K1000.B. One day later, Samsung released the world's first 1.5-Tbyte HDD, high-end member of the 7200.11 product family, which was scheduled to enter production in August. At 375 Gbytes/platter, it hits a new bit-packing peak for PMR (perpendicular-magnetic-recording) technology. That same generation of magnetic recording translates to 0.5-Gbyte, 5400- and 7200-rpm, 2.5-in. HDDs, which won't appear until some time in the fourth quarter.

> "Hitachi's accomplishment didn't remain sole-sourced long, of course.

And what about the SSD (solid-state-drive) alternative? Although SSDs lag their HDD counterparts on both absolute capacity and cost/gigabyte metrics, suppliers continue striving to at least maintain pace with the rotating-storage mainstay. Witness, for example, Samsung's 128-Gbyte SSD announcement. Samsung accomplishes this 2.5-in.-form-factor feat by means of MLC (multilevel-cell, also known as 2-bit-per-cell) NAND-flash memory, which roughly doubles the amount of storage capacity achievable for a given amount of silicon area on a given process lithography.

—by Brian Dipert

▶www.edn.com/briansbrain.

▶For the full post, go to www.edn.com/080904b2.

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ANALOG DEVICES

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Pentek's Rodger Hosking: next-generation-radio architect

Rodger Hosking is vice president and co-founder of Pentek Inc, where he is responsible for new-product definition, technology development, and strategic alliances. With more than 30 years' experience in the electronics industry, he has authored hundreds of articles about software radio and digital-signal processing. He designed the first commercial direct-digital-frequency synthesizer and holds patents in frequency synthesis and FFT (fast-Fourier-transform)-spectrum-analysis techniques. Hosking has a bachelor's degree in physics from Allegheny College (Meadville, PA) and both bachelor's and master's degrees in electrical engineering from Columbia University (New York).

What are the technical challenges that you face in high-performance-data-acquisition- and software-radio-product development?

A Complexity of the silicon devices, coupled with high component density and power dissipation, pushes the limits of PCB [printed-circuit-board] design, mechanical packaging, and thermal-management technology. Gigabit serial links impose strict layout rules for matching lengths and impedances of differential-signal pairs. Testing and validation of new designs requires not only hardware expertise, but also a significant software effort because of the complexity and inaccessibility of hardware test points. Drivers and software libraries offered by the COTS [commercial-off-the-shelf] vendors to support customer-development efforts need to support multiple operating-system environments and require more testing, qualification, and documentation than ever before.

All of these factors lead to longer development cycles while the rate of new-technology-device introductions is increasing. This [combination of factors] leads to shorter life cycles for each product, even though development costs are higher.

As you look ahead for the next few years, which technologies and applications present the most interesting opportunities?

A FPGAs have created a major shift in COTS-product offerings for data acquisition and software radio by offering critical functions, including fast and flexible I/O resources, DSP engines, configurable logic and RAM, gigabit serial interfaces, and built-in microcontrollers. All of these features will become more powerful in next-generation FPGAs. Monolithic ADC and DAC technology will continue to advance both resolution and sampling rates while taming power dissipation with new silicon techniques.

These trends will support small, complete, system-level solutions close to the antennas and sensors. They will include acquisition, generation, upconversion and downconversion, modulation and demodulation, analysis and detection, buffering and forwarding, and local supervisory and decision-making functions. High-speed gigabit links will connect these autonomous subsystems to a central facility through dedicated paths or over the Internet.

As a COTS-board manufacturer, how do you prevent the interoperability issues when designing for today's rival fabric-interconnection standards?

A The most successful tactic has been to follow the standards as closely as possible and declare each level of compliance your product supports. A series of simple example programs demonstrating operation of the basic messaging types can be extremely useful for interfacing with products from other vendors.

Which engineering talents are most important to Pentek, and how do you find and retain them?

A Fifteen years ago, we had one software engineer for every three hardware engineers. That ratio is now exactly reversed due to the complexity of the products and the need to provide higher-level tools to our customers. Our most capable FPGA designers started as hardware engineers with a flair for algorithms, DSP, and software tools. More than ever, technical writers need to be capable engineers with specific expertise in the area of technology they are documenting but not so close to it that they overlook the need to explain some of the basics in our manuals. Customer-support engineers need a special blend of technical expertise, patience, and empathy to help customers become successful, even if it is their first exposure to this complex technology.

Retaining engineers is difficult because each one is uniquely qualified and motivated, but tasking them with several areas of engineering responsibilities often proves to be a successful strategy.

What motivated you to select electrical engineering and the high-tech industry as a profession?

A As a very small child, I was always fascinated with anything that had to do with electricity. Later on, I became an avid electronics hobbyist, building hundreds of my own projects inspired by magazine articles and books. For me, a career in electronics was a no-brainer.

What activities do you pursue for relaxation outside your high-tech work environment?

A Outside work, I spend my time running, rollerblading, ballroom dancing, watching old movies, and listening to music from the '30s and '40s.

—Interview conducted and edited by Warren Webb

RAQ's

Rarely Asked Questions

Strange stories from the call logs of Analog Devices

Lock Down That Noise — Don't Let It Escape

Q. How can I prevent switching-mode power supply noise from devastating my circuit performance?

A. With great difficulty — but it can be done.

Switching-mode power supplies are inherently the noisiest circuits imaginable. A large current from the supply is being turned on and off at high frequency with very fast dI/dt. There are inevitably large fast voltage and current transients.

The only way to prevent interference to sensitive circuitry in the system is to keep the transients within the converter. We cannot stop switching large currents inside it, but we can, and must, prevent the transient currents and voltages from escaping. Start by grounding all the terminals of the converter at AC.

Capacitors block DC but have low impedance at AC, so they should be ideal for this purpose. In theory, if we place a large capacitor between the converter input and its ground, the input will keep the capacitor charged and the transient currents will flow in the capacitor and not from the power source. A similar output capacitor absorbs transients and sources steady DC.

Unfortunately when we actually build such a system it is common to find much more noise than we can tolerate in the input and output circuits - what can be wrong?

If the capacitor is placed some distance from the converter, the impedance, resistive and inductive, of its connection to the converter will be large enough to prevent it from working properly; if it is chosen badly it will have higher impedance

than the basic $1/2\pi fC$ formula predicts; and if it shares its ground path with other circuitry the noise in the common ground impedance will be disruptive.

Add to these effects the less important, but still damaging, consequences of external currents induced by fast-changing magnetic and electrostatic fields, and even electromagnetic radiation, from within the converter, and it is obvious that preventing converter noise is not simply a matter of placing a couple of random capacitors on its input and output.

Silencing a DC-DC converter requires systematically finding all the possible paths by which noise can escape from it, and ensuring that they are all locked down. The linked article discusses how this may be done.

Of course before we start we must choose or design the converter itself to have minimal external noise. This is a separate issue which may be discussed in a future RAQ.

To Learn More About Power Supply Noise

Go to: http://rbi.ims.ca/5721-101

Contributing Writer James Bryant has been a European Applications Manager with Analog Devices since 1982. He holds a degree in Physics and Philosophy from the University of Leeds. He is also C.Eng., Eur.Eng., MIEE, and an FBIS. In addition to his passion for engineering, James is a radio ham and holds the call sign G4CLF.

Have a question involving a perplexing or unusual analog problem? Submit your question to: raq@reedbusiness.com

For Analog Devices' Technical Support, Call 800-AnalogD

BY BONNIE BAKER

Transimpedance-amplifier stability is key

A variety of precision applications sense light and convert that information into a useful digital word. At the system's front end, a preamplifier converts the photodiode's current-output signal to a usable voltage level. **Figure 1** shows the front-end circuit of this system, which comprises a photodiode, an operational amplifier, and a feedback network. The transfer function of this system is:

$$V_{OUT} = \frac{I_{SC} \times R_F}{1 + 1/(A_{OL}(j\omega) \times \beta)},$$

where $A_{OL}(j\omega)$ is the open-loop gain of the amplifier over frequency; β is the system-feedback factor, equaling $1/(1+Z_{IN}/Z_F)$; Z_{IN} is the distributed input impedance, equaling $R_{PD} \| j\omega(C_{PD}+C_{CM}+C_{DIFF})$; and Z_F is the distributed feedback impedance, equaling $R_F \| j\omega(C_{RF}+C_F)$.

A good tool for determining stability is a Bode plot. The appropriate Bode plot for this design includes the amplifier's open-loop gain and the $1/\beta$ curve. System elements determining the noise-gain frequency response are the photodiode's parasitics and the operational amplifier's input capacitance, as well as R_F, C_{RF}, and C_F in the amplifier's feedback loop.

Figure 2 shows the frequency response of the $1/\beta$ curve and the amplifier's open-loop-gain response: $f_p = 1/(2\pi(R_{PD} \| R_F)(C_{PD}+C_{CM}+C_{DIFF}+C_F+C_{RF}))$, and $f_Z = 1/(2\pi(R_F)(C_F+C_{RF}))$. The $A_{OL}(j\omega)$ curve intersects the $1/\beta$ curve at an interesting point. The closure rate between the two curves suggests the system's phase margin and, in turn, predicts the stability. For instance, the closure rate of the two curves is 20 dB/decade. Here, the amplifier contributes an approximately −90° phase shift, and the feedback factor contributes an approximately 0° phase shift. By adding the $1/\beta$ phase shift from the $A_{OL}(j\omega)$ phase shift, the system's phase shift is −90°, and its margin is 90°, resulting in a stable system. If the closure rate of these two curves is 40 dB/decade, indicating a phase shift of −180° and a phase margin of 0°, the circuit will oscillate or ring with a step-function input.

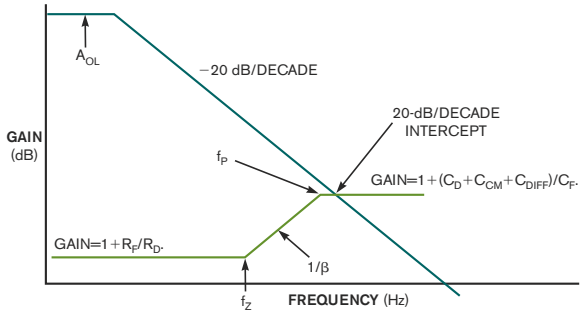
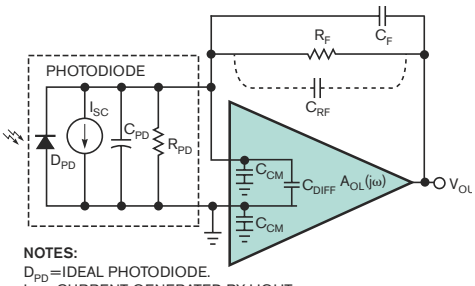


Figure 2 The closure rate between the open-loop-gain frequency response and the feedback-gain response is 20 dB/decade.



NOTES:
D_{PD}=IDEAL PHOTODIODE.
I_{SC}=CURRENT GENERATED BY LIGHT.
C_{PD}=DEVICE CAPACITANCE.
R_{PD}=DEVICE PARALLEL RESISTANCE.
C_F=FEEDBACK CAPACITOR.
R_F=FEEDBACK RESISTOR.
C_{RF}=FEEDBACK-RESISTOR PARASITIC CAPACITANCE.
C_{CM}=COMMON-MODE-AMPLIFIER CAPACITANCE.
C_{DIFF}=DIFFERENTIAL-AMPLIFIER CAPACITANCE.
$A_{OL}(j\omega)$=AMPLIFIER OPEN-LOOP GAIN.

Figure 1 This transimpedance photosensing circuit comprises a photodiode, an operational amplifier, and a feedback network.

One way to correct circuit instability is to add a feedback capacitor, C_F, or to change the amplifier to have a different frequency response or different input capacitance. A conservative calculation that allows variation in amplifier bandwidth, input capacitance, and feedback-resistor value places the system's pole of $1/\beta$ at half the frequency where the two curves intersect:

$$C_F = \left[2 \times \sqrt{\frac{(C_{PD}+C_{CM}+C_{DIFF})}{2\pi R_F f_{GBW}}}\right] - C_{RF},$$

where f_{GBW} is the gain-bandwidth product of the amplifier. In this design, the system's phase margin is 65°, and the step function's overshoot is 5%. EDN

REFERENCE

1 Baker, Bonnie, "The eyes of the electronic world are watching," *EDN*, Aug 7, 2008, pg 24, www.edn.com/article/CA6582850.

Bonnie Baker is a senior applications engineer at Texas Instruments and author of A Baker's Dozen: Real Analog Solutions for Digital Designers. *You can reach her at bonnie@ti.com.*

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Go to www.edn.com/080904pry for an expanded version of this article.

Prying apart a portable audio player

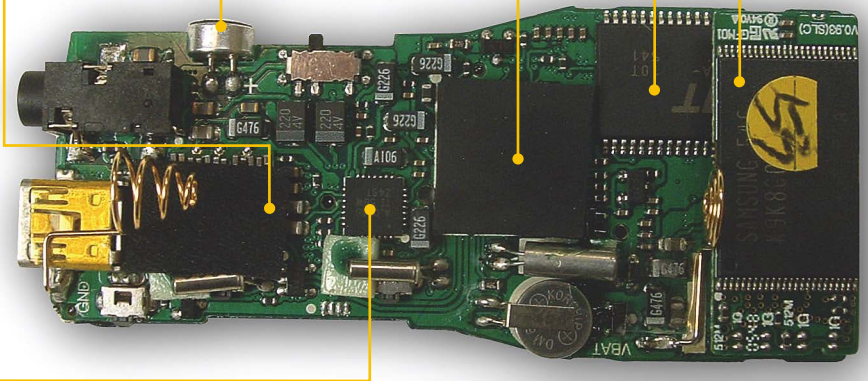
Free after $65 rebate with free shipping. That's the deal that routed a refurbished Sandisk Sansa M250 from Newegg to my front door last summer. I suspected it would make a fine Prying Eyes patient, and, as it turns out, I was right. Let's see what's inside, shall we?

The system's "brains" consist of an ARM9-based and USB2-support-inclusive Telechips TCC770. The Sansa M250's built-in microphone for voice recording and subsequent playback likely harnesses the CPU's ADPCM (adaptive-differential-pulse-code-modulation)-audio-codec support.

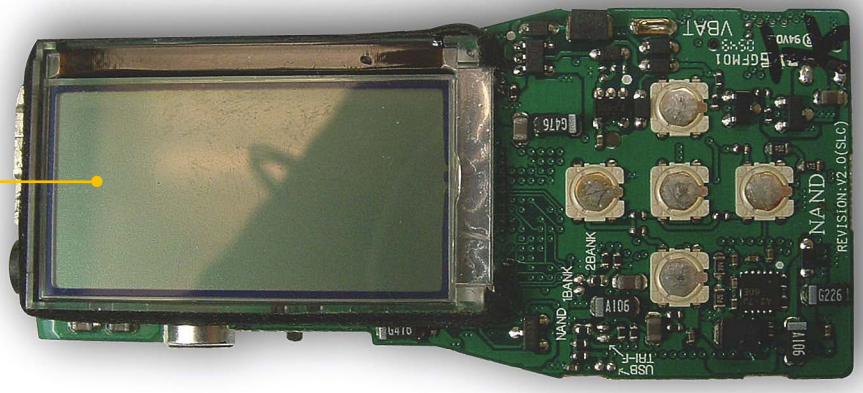
The Sansa M250 embeds a single battery-backed, 16-Mbit Elite Semiconductor M12S16161A SDRAM, supplementing the 64 kbytes of SRAM within the Telechips TCC770. Among other functions, the SDRAM probably acts as a "shadow" for the direct execution of system code that the NAND-flash memory stores.

Above the SDRAM and an intermediary piece of cushioning foam are two 1-Gbyte Samsung K9K8G08U0M NAND-flash-memory devices on a double-sided daughtercard. This modular arrangement gives Sandisk the flexibility to leverage a common primary-PCB design across multiple Sansa M200 family proliferations—having 512-Mbyte, 1-Gbyte, and 4-Gbyte capacities—and to source NAND-flash memories in multiple IC-density, architecture, and supplier variations.

Texas Instruments' TLV320AIC-23B two-channel codec—that is, ADC and DAC—with headphone amplifier is another notable IC in this design; however, the player doesn't fully harness the chip's 24-bit maximum per-channel sample size and 96-kHz peak sample rate.



The Sansa M250 uses the Philips (now NXP Semiconductors) TEA5767HN FM radio IC for playback only—that is, the Sandisk unit offers no support for live recording and later listening. The lack of a discrete antenna embedded within the Sansa M250's plastic case probably indicates the use of the headphone wire for this function.



The Telechips TCC770 advertises limited-codec image-decoding support: JPEG pictures and MPEG-4 Simple Profile video clips. The Sansa M250 collateral makes no mention of image-file capabilities; then again, the unit's 128×64-pixel monochrome LCD wouldn't really do them justice, anyway.

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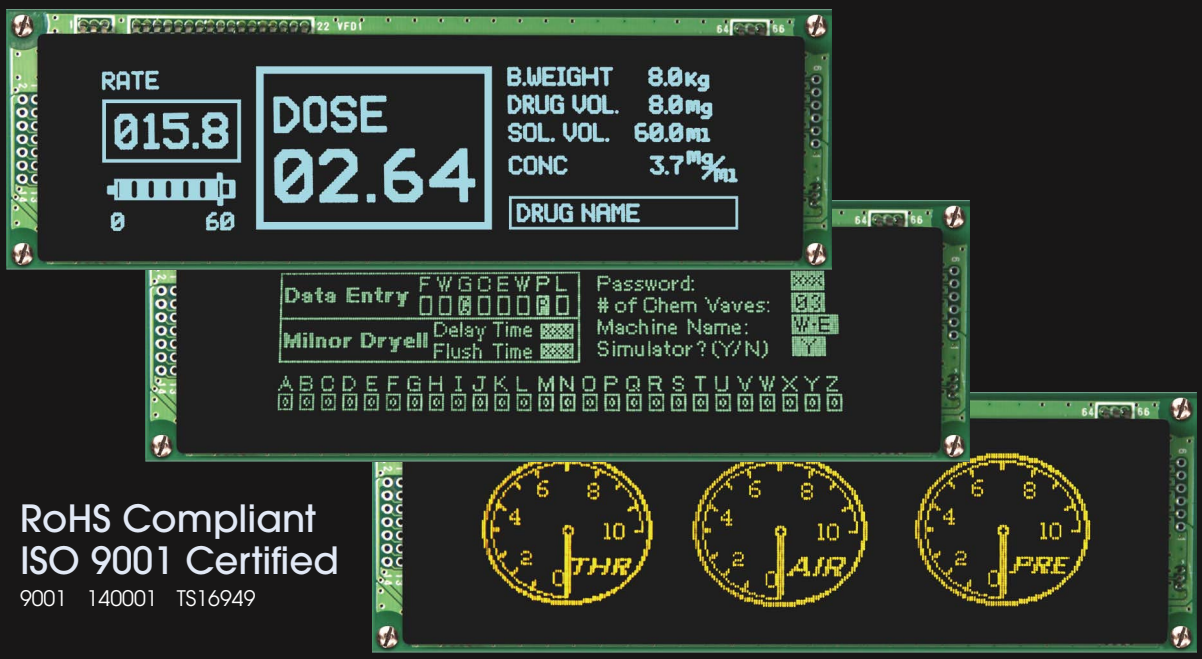

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SHEDDING LIGHT ON EMBEDDED DEBUGGING

EMBEDDED DEBUGGING GETS A LOT OF ATTENTION FOR BEING A SCHEDULE AND RESOURCE HOG, BUT THERE MAY BE MORE TO IT THAN JUST FIXING BAD SOFTWARE.

For each year of *Embedded Systems Design*'s annual market survey of embedded-system developers, the single most requested area of improvement for design activities is debugging tools (**Reference 1**). The percentage of respondents making this request has remained steady at around 32% throughout the three years of the survey. In contrast, the percentage of respondents seeking improved programming tools has dropped from a high of 25% to 10%. Determining why the evolution of modern debugging tools is failing to hit the mark as well as software-programming tools do is worth exploring—especially when the surveys each year also confirm that the testing-and-debugging phase continues to be the one that consumes the largest amount—24%—of the project schedule. The third standout request for improvement in all three years' surveys is the project-management function of scheduling (see **sidebar** "COCOMO and evidence-based scheduling").

One explicit aspect of engineering is to create systems that perform and deliver a practical approach to a problem. Software-programming tools focus on the creation side of software engineering. The survey results suggest that programming tools are on the right path toward improving productivity for the creation of system code to solve problems. But the failure of debugging tools to trend downward as a primary concern alongside programming tools suggests that software-debugging tools are not merely extensions of programming tools that help developers correct mistakes or incorrect coding.

There is a less obvious, almost implicit aspect of engineering—that designers must not only design systems that perform some desirable function, but also eliminate or mitigate undesirable behaviors that may result from uncertainty and variability in the environment, so that the system behaves consistently across a range of operating conditions. This hidden side of engineering potentially provides insight into the challenges facing software-debugging tools, especially for embedded-system designers. In addition to dealing with processor-architecture practical constraints for performance, function, communication, latency, and power consumption, embedded systems often have to deal with real-world interfaces that may exhibit behaviors that are more difficult to predict or characterize completely across the whole range of usage scenarios.

If debugging were only about finding and correcting software-logic errors, an instruction-set simulator in conjunction with cycle-accurate simulators might provide enough visibility into the behavior of embedded systems to support debugging. Such simulators are available for most processor architectures and software-development-tool suites. Simulators can also stop the system and examine any parts of the simulated system. Unfortunately, these types of simulators usually cannot provide complete visibility into the exact interaction and latency of the memory, bus architectures, peripherals, sensors, and actuators. Such fidelity would make the simulators operate even slower than they already do.

System-level simulators, such as the virtual-system-prototype tools from Vast and the Simics virtual platform from Virtutech, have the potential to go beyond the software-execution engine and simulate the interactions of the other parts of the system. These types of development tools can enable software developers to work on a target before the physical hardware is available; they also can assist developers with system integration and testing efforts by supporting system-level fault injection and incremental integration in parallel to other development activities. These types of systems can act as precursors or support to hardware-in-the-loop simulations for high-end, complex systems. These tools support prebuilt systems and assembling a system from prebuilt parts or blocks. With additional tooling, they offer the ability to build new components to integrate into the system.

One hurdle system-level simulators face is cost, which can exceed by many thousands of dollars the price of available processor-centric simulators. It is possible that debugging tools are not following the downward trend in the surveys with programming tools not because they are failing to meet the functional needs of embedded-system developers, but rather because the higher-end

AT A GLANCE

- Engineering embedded systems is not just about making them perform some behavior but preventing them from exhibiting undesirable behavior.
- Designers may be using debugging tools as design aids because there are no other better means for doing the job.
- Debugging embedded systems is a cross-disciplinary activity, crossing hardware, software, and domain-expertise boundaries.

COCOMO AND EVIDENCE-BASED SCHEDULING

Realistic schedules are keys to creating good software. Deadlines that are too tight create avoidable stress sources that could lead to shipping an incomplete project. Recognizing that a deadline is too tight forces you to focus on the best or the most important features first, and it helps you to make the right decisions about what to incorporate into the final product. There have been a number of approaches to helping project managers produce more accurate schedules that trade off features, cost, and time for software-development projects.

One such approach is COCOMO (constructive-cost model), an algorithmic-software-cost-estimation model that applies a regression formula with historical project data and current project characteristics. Software engineer Barry Boehm first published the model in 1981. The COCOMO II model incorporates changes in software development over the years to estimate the cost, effort, and schedule when planning new software-development projects. The COCOMO II model is available to the public from the University of Southern California Center for Systems and Software Engineering Web site (Reference A).

COCOMO II comprises application-composition, early-design, and post-architectural submodels that provide increasing fidelity according to how far the project-planning and -design process has proceeded. COCOMO II can assist with setting project budgets and schedules; making software-cost and schedule-risk-management decisions; making trade-offs among software cost, schedule, functions, performance, and quality factors; and deciding which parts of a software system to develop, reuse, lease, or purchase. A key factor in continuing to improve the predictive accuracy of COCOMO II is good data. The COCOMO II research group is asking for help from the software industry to collect data from development projects; the data collection will enable the availability of a more accurate predictive model for estimating software-project costs.

Another approach for incorporating historical data into the schedule modeling appears in a posting by Joel Spolsky, chief executive officer of Fog Creek Software, on evidence-based scheduling (Reference B). The article describes the approach for the model in a general fashion, although Fog Creek uses the model in its FogBugz commercial product. The first step is scheduling in chunks that you measure in hours–for example, no more than 16 hours to ensure the estimator has actually thought about the steps necessary to complete a task. By keeping time sheets, you can compare estimates with the actual results from each developer and establish estimate-scaling velocities that will not only help you improve your estimates over time, but also provide you a model for Monte Carlo simulation to calculate and chart the probability that you will be able to ship by any given date. Armed with the charted probable-shipping dates, you can explore how shifting the priorities of different features or including changes in scope may affect the schedule.

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A "COCOMO II," http://sunset.usc.edu/csse/research/COCOMOII/cocomo_main.html.

B Spolsky, Joel, "Evidence Based Scheduling," *Joel on Software*, Oct 26, 2007, www.joelonsoftware.com/items/2007/10/26.html.

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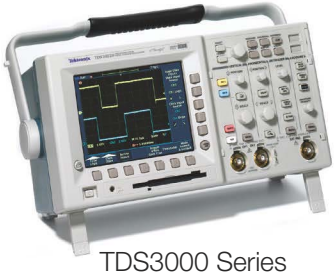

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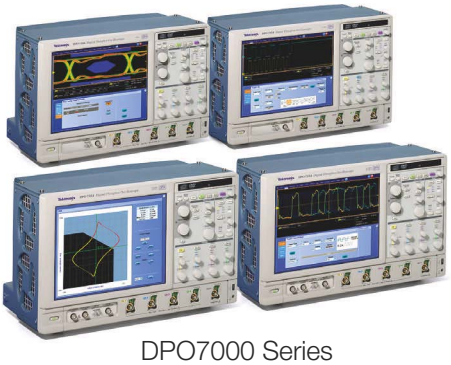

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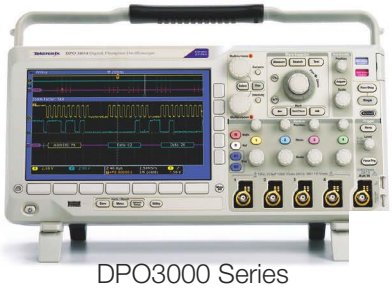

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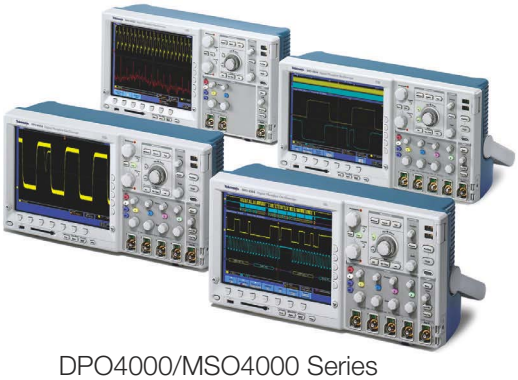

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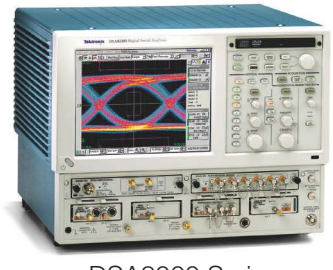

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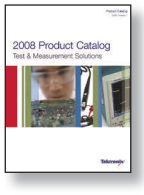

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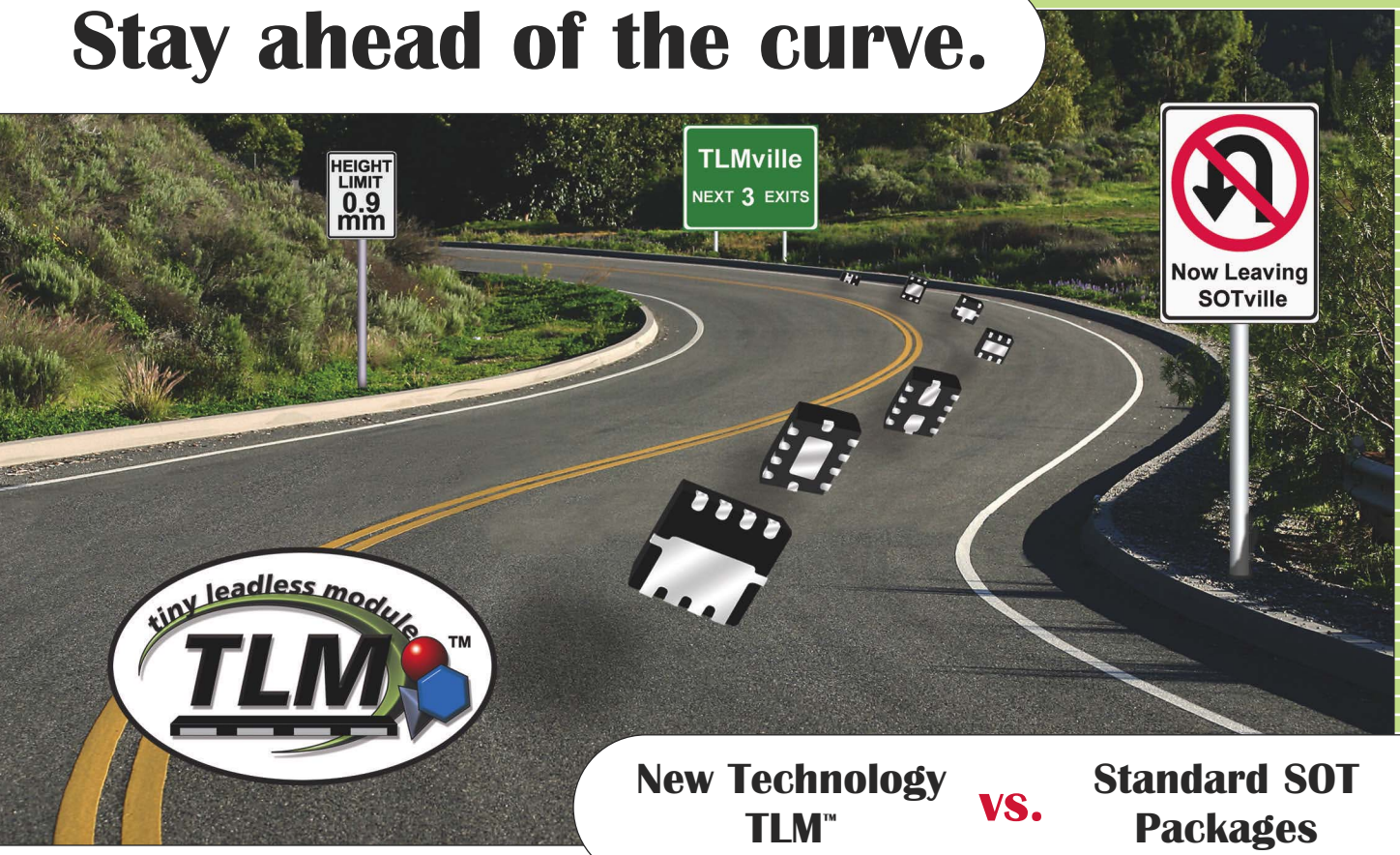

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CTLSH1-40M832D	1.0	40	Dual, Schottky	3 x 2 x 0.9	TLM832D
CTLSH2-40M832	2.0	40	Single, Schottky	3 x 2 x 0.9	TLM832
CTLSH3-30M833	3.0	30	Single, Schottky	3 x 3 x 0.9	TLM833
CTLSH5-40M833	5.0	40	Single, Schottky	3 x 3 x 0.9	TLM833

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Central Type No.	I_C (A)	V_{CBO} (V)	Description	TLM Size L x W x H (mm)	Package
*CTLT3410-M621	1.0	40	Low $V_{CE(SAT)}$, NPN	2 x 1 x 0.8	TLM621
*CTLT7410-M621	1.0	40	Low $V_{CE(SAT)}$, PNP	2 x 1 x 0.8	TLM621
CTLT853-M833	6.0	200	High Current, NPN	3 x 3 x 0.9	TLM833
CTLT953-M833	5.0	140	High Current, PNP	3 x 3 x 0.9	TLM833

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Central Type No.	Transistor		Rectifier		TLM Size L x W x H (mm)	Package
	I_C (A)	V_{CBO} (V)	I_F (A)	V_{RRM} (V)		
CTLM1034-M832D (NPN)	1.0	40	1.0	40	3 x 2 x 0.8	TLM832D
CTLM1074-M832D (PNP)	1.0	40	1.0	40	3 x 2 x 0.8	TLM832D

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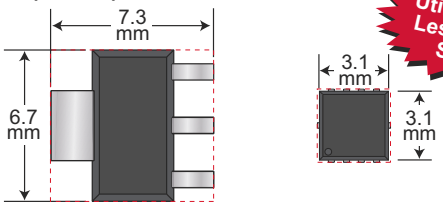

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debugging tools with the needed functional support still exceed some critical cost threshold. It is interesting to note that this cost threshold is lower than that for hardware-design tools, even though most software-development tools will likely support more of the additional complexity in new systems.

The last decade has seen serious erosion in royalty-based operating-system- and development-tool-license models. The growing success of Linux as an operating system in embedded systems is due largely to the cost advantage of using open-source software. Additionally, many embedded-system tools from silicon providers have adopted the open-source Eclipse platform to host their development tools, which substantially reduces the cost of building these tools, simplifies configuring their tools by the end user, and allows them to focus their engineering effort on the features of the tools rather than the look and feel of the host environment. This observation is not to say that debugging tools have not followed the same downward trend in pricing. At the extreme, many processor vendors offer small evaluation kits that allow developers to experiment with the systems for much less than $100. Indeed, many development kits that cost hundreds of dollars today include features you would find a decade ago only in much costlier tool sets.

As on-chip-debugging circuitry expands on contemporary processor architectures, the industry may continue to see the higher-end-debugging functions finding their way into lower-cost development-tool kits. Many processors, including small, 8-bit processors, contain some proprietary on-chip-debugging circuitry. "The on-chip-debug system is one of the most complex circuits in the chip because it has to non-intrusively interconnect with all of the subsystems," says Dag Arne Braend, AVR-development-tool director at Atmel. "And it has been difficult to justify incurring the extra cost for this complexity for something that many systems will never use in field devices."

Real-time trace appears to be the next emerging on-chip-debugging capability moving down the processor hierarchy. Processors using ARM cores with an ETM (embedded-trace macrocell) enable the downloading of instruction and data traces from the processor. The

THE LAST DECADE HAS SEEN SERIOUS EROSION IN ROYALTY-BASED OPERATING-SYSTEM- AND DEVELOPMENT-TOOL-LICENSE MODELS.

Cortex-M3 core supports a new real-time-trace capability. Trace enables reverse-order instruction execution, which more simulators are supporting. The Green Hills Software Multi Time Machine debugging suite enables developers to swap between on-chip debugging and simulator debugging to support simulated reverse-order execution.

IEEE-ISTO 5001-2003, the Nexus 5001 Forum open industry standard for a global embedded-processor-debugging method, provides a general-purpose interface for the software development and debugging of embedded processors. The initial focus of the Nexus 5001 Forum was automotive power-train applications, but its result has evolved to become a general-purpose standard. The Nexus 5001 Forum membership spans the semiconductor, development-tool, and automotive-electronics industries. As the cost of silicon continues to drop and on-chip-debugging interfaces and functions become standard, processor providers will likely flow high-end on-chip-debugging capabilities from high-end processors to lower-end processors to provide even more on-chip visibility. This step will become necessary to gain design wins.

DESIGN AID

John Lambert, chief executive officer of Virtutech, offers an immediate possible mitigating factor for the higher costs in favor of system-level-simulation tools. "A development team usually acquires our platform to support either the front or the back end of its current proj-

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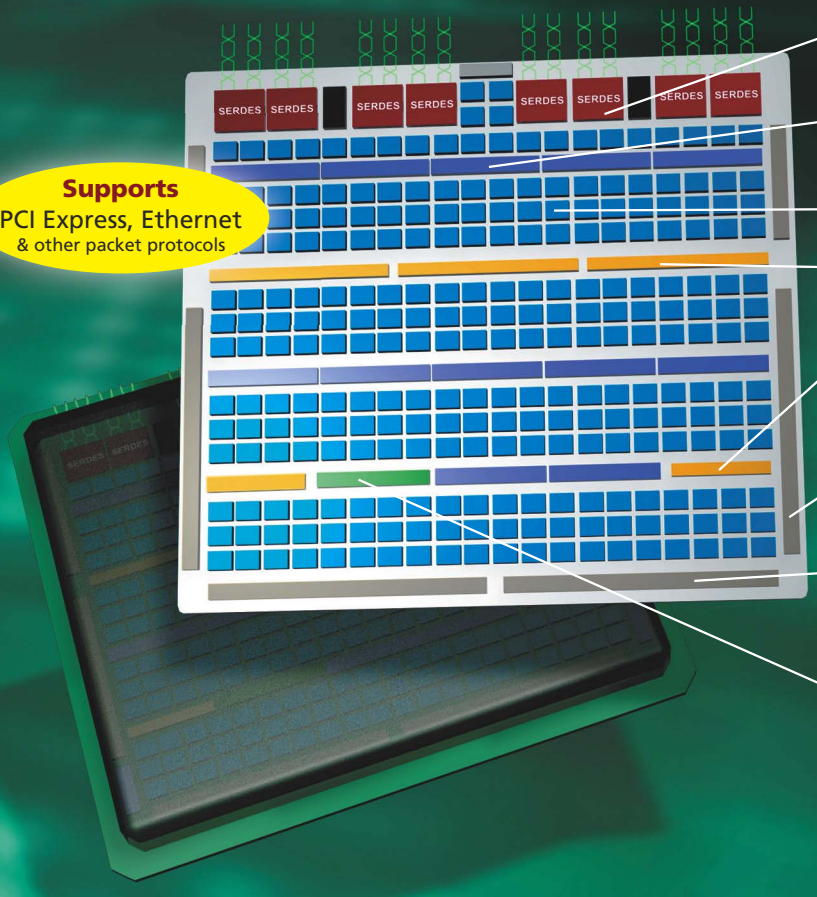

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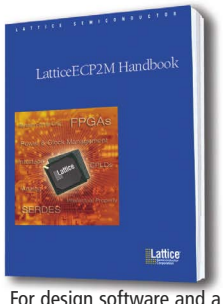

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ect, but once the team uses the tool, it more fully realizes its value and uses it at both ends of the design cycle in future projects," he says.

This theory exposes another possible disconnect in what embedded-system designers mean when they say they need better debugging tools. A primary function of debugging tools is to provide visibility into the state of the system during runtime. When a system includes complex interfaces, sensors, and actuators, a debugger may be the most expedient tool available for examining these external systems' functions because accurate signal generation for all of the tightly coupled subsystems is a major challenge. Therefore, one reason you might call them debugging tools instead of design aids is that the capabilities of the tools are unusable until the system-integration phase of a project, when debugging is well under way.

Looking at debugging tools as design aids provides a valuable perspective, especially when working with closed-loop-control systems where the outputs affect the inputs of a system. It can be challenging to verify the behavior of closed-loop-control systems. I have used end-system software and sensor hardware to characterize and validate how an automatic-gain-control algorithm worked with a sensor across a range of expected circumstances (**Reference 2**). There was no way to simulate this condition or even test for something like it in a pure software-debugging environment because there is no accurate model for the sensor. As a result, I discovered an unknown characteristic of the sensor before it was too late.

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ONE REASON YOU MIGHT CALL THEM DEBUGGING TOOLS INSTEAD OF DESIGN AIDS IS THAT THE CAPABILITIES OF THE TOOLS ARE UNUSABLE UNTIL THE SYSTEM-INTEGRATION PHASE OF A PROJECT.

A second example involved taking the system-integration-test data and running it through a spreadsheet program to analyze whether the closed-loop-control algorithm was performing properly. Again, no amount of software simulation or design effort could account for actually hooking the equipment together and collecting the data; it was more cost-effective to run the tests during integration than to try to create one-time-accurate models of the prototype system. However, I did use the information I learned about the system behavior to build simulation models for the next-generation-development work.

Another characteristic of debugging embedded systems is that problems are not necessarily solely from software errors. However, because it is much more cost- and schedule-effective to fix most problems in software, designers usually implement a software fix to resolve problems. However, making and recording a fix as a software change belies the amount of cross-discipline cooperation necessary to find, diagnose, and determine an acceptable resolution. In fact, many embedded-system-debugging problems are cross-disciplinary, requiring understanding and expertise of the system hardware, software, and domain-specific constraints. This situation does not pose a problem if the person doing the system-integration testing happens to be an ex-

pert in all three of these disciplines, but those types of people are rare indeed.

Because of the cross-disciplinary nature of debugging embedded systems, debugging tools and engineering services have an opportunity to fill a void. Just because a debugging tool provides a specific type of visibility into the system does not mean that developers will use that feature. David Kleidermacher, chief technology officer at Green Hills Software, agrees. "Too many options in tools require a larger learning curve for developers, [which] results in a low adoption rate of many of those features," he says. Developers tend to use the simplest features due to time pressure, and developers adopt these advanced features more as part of a lesson they learned from previous projects. Partly in response to this realization, Green Hills added an "always-on" trace capability to its Multi Time Machine debugging tool; the trace has become more useful to developers because the default condition costs the developer practically nothing, requires no learning curve to use, and is more effective than explicitly turning on the trace-capture function.

Another challenge facing developers debugging embedded systems is setup and configuration of the testbench. This issue is a low-cost, high-value concern that many tool providers are trying to address in their tool sets. The power supply for many evaluation boards now comes through the USB connection, which greatly simplifies the power setup for using those boards. The interfaces to send commands and collect data between the embedded system and the host system are now simpler to use, and there is talk of using wireless interfaces for debugging systems in the near future. Many development-tool sets provide a preconfigured setup and allow developers to test the board to confirm that it and its tools are working properly in a known circumstance. Reid Tatge, a technical fellow at Texas Instruments, explains that a goal of the company's development tools is to make embedded development look like the development of "wintel" systems—those based on Intel microprocessors and Microsoft Windows operating systems—to ease the learning curve for designers to use their embedded processors.

Micrium's µC/Probe aims to make it easier for developers to quickly visualize what is going on in their systems. The tool consists of two pieces of software—one that runs on the host system and performs the data analysis and display and one that acts as a code stub that you load on the target system. The stub manages I/O and resource queries as well as communication with the host system. Although it is an intrusive form of instrumenting the embedded-system code, it provides runtime access to the system without halting your system. The tool is available for around $1000.

National Instruments' LabView provides strong visualization support and includes a graphical-programming capability. It also includes built-in measurement and analysis functions that it organizes around application domains so that developers can select which capabilities to use. The debugging visualizations are well-suited for data-flow execution models. Prices for tool sets that integrate hardware, software, and domain-specific functions start at around $1000 but can exceed $10,000 if you need to add on a heavy amount of domain-specific tools.

This type of pricing flexibility illustrates a challenge for many tool providers; customers want to pay for only the right level of visibility based on different touch points. For example, some developers target an operating system and do not concern themselves with the details of the underlying processor architecture.

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Other developers target the instruction-set architecture. Still others worry about lower-level interactions, such as those in the architecture layer, which connects all of the resources in the system.

Even when the tools provide the visibility a designer needs, knowing what to look for is another hurdle because the communication link between the on-chip system and the host system limits the amount and type of captured data that can make it to the host system for real-time and post-runtime analysis. Additionally, processor vendors do not always expose features to the public that they implement on a chip; they may choose to hide those features because the features are experimental and vendors are not ready to provide robust, production-level support for them. Internal tools and expert field-application-engineering services, however, can take advantage of those hidden resources. But it is a far cry from having a tool that an expert can use in a limited situation to making that tool robust and usable across a wide range of scenarios and expertise levels. Unfortunately, engineering services are labor-intensive and expensive—far exceeding the cost threshold of most software-development budgets except in the most dire of troubleshooting scenarios.

To continue evolving, debugging tools require correlated input from hardware, software, and domain experts. In some situations, there is a negative incentive for customers of processor or tool providers to share their hard-learned lessons. If they share the key lessons with tool developers, they may shorten the learning curve necessary for competitors and avoid incurring the scheduling and engineering-expertise cost of learning how to make the embedded system work in a certain way. The experience of field-application engineers can help give tool developers the necessary insight to make debugging tools more useful in these cases.

Embedded systems have for decades been implementing multiprocessor designs, but new opportunities for tightly coupled multicore and multiprocessor systems continue to emerge. Additionally, a growing number of embedded systems are using even more sensors in their systems so that they can adequately take on and manage more complex behaviors. These trends in emerging embedded systems will require debugging tools to deliver even stronger coherency and related visualization features because the interactions between the subsystems will continue to become more complex than ever before. **EDN**

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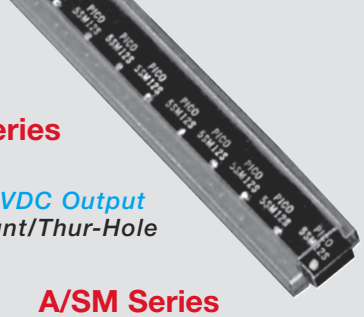

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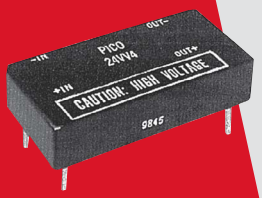

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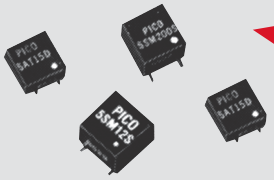

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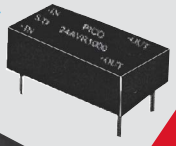

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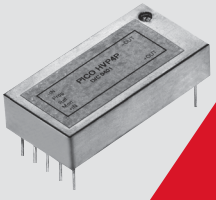

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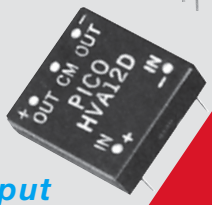

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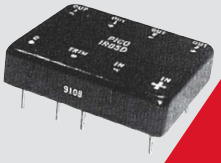

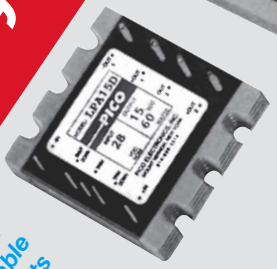

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BY RICK NELSON • EDITOR-IN-CHIEF

HANDCRAFTED ANALOG GETS AUTOMATED ASSIST

EDA TOOLS ADDRESS SIMULATION, VERIFICATION, AND LAYOUT FOR MIXED-SIGNAL DESIGNS.

Analog simulators and design-capture tools have a venerable history in the EDA market, having long added some Spice to their digital-simulation counterparts. When it comes to converting simulations to sine waves and silicon, however, analog-EDA tools fall short of what has been possible in the digital domain. That scenario is beginning to change. Tools are emerging from traditional digital-EDA providers that support the fabrication of analog functions in nanometer-geometry digital processes. In addition, foundry-specific tool kits are easing the implementation of analog, RF, and high-voltage functions in analog processes.

Designers cannot expect smooth sailing, though; full automation of analog- and mixed-signal design remains elusive. Even analog-Spice engines may run out of steam as chips become more complex, requiring excessive times for full-chip simulation, even with fast-Spice implementations. Nevertheless, vendors are working on multiple fronts to bring automaton to the traditionally handcrafted analog-design task.

One way to deal with analog design is to reformulate analog problems as computational ones. Justin R Rattner, vice president and chief technology officer at Intel, suggested that approach, digitally assisted analog, during this year's DAC (Design Automation Conference) keynote address (**Reference 1**). Not all problems are amenable to digital computational solutions, however. You can't readily "calculate" a 120V signal level, no matter how many 45-nm digital transistors you throw at the problem. And, apart from voltage and current levels, the need for analog functions isn't going away. As Texas Instruments Senior Vice President Gregg Lowe points out, the transition to digital—for instance, music's transition from vinyl to MP3—results in an increase in analog content (**Reference 2**).

The need for more analog content mandates better analog-design tools. Mar Hershenson, vice president of product development at Magma Design Automation's custom-design-business unit, describes analog design as it has occurred over the last 20 years as the work of artists, with engineers manually designing op amps and other analog functions. As if analog design weren't difficult enough, she adds, integrating the analog and the digital portions of a mixed-signal design can take weeks. Further, for every process node, analog-system engineers must manually re-create designs.

And even ICs that are functionally digital—that is, producing no signals other than zeros or ones—are exhibiting behavior that requires analog-design and -test techniques. That situation is particularly true of the high-speed serial interfaces that let chips communicate with the outside world.

IP AND ANALOG BEHAVIOR

The term *analog* conjures up visions of op amps and data converters, but, explains Navraj Nandra, director of marketing for mixed-signal IP (intellectual property) at Synopsys, "The speeds of today's chips' serial-digital-I/O lines ensure that analog effects come into play" even in

ostensibly all-digital parts. Complicating matters, he says, is that pure-analog companies have the luxury of implementing functions in processes optimized for analog circuitry. In contrast, companies making digital chips want to implement their high-speed I/O in standard deep-submicron digital processes—with all the attendant process-variation and signal-integrity issues.

Synopsys addresses serial-I/O-design problems with its DesignWare IP to implement functions, such as USB 2.0, DDR2/3 memory, SATA (serial-advanced-technology-attachment), and PCIe (peripheral-component-interconnect-express) 2.0 interfaces. The DesignWare PCIe 2.0 product, for example, includes the PHY (physical-layer interface), operating at 5 Gbps, as well as a digital controller and verification IP. Nandra notes that Synopsys has successfully produced a USB 2.0 PHY in 65-nm processes at fabs Chartered Semiconductor, Samsung, and IBM—all with a single GDSII (graphic-design-system II) file with no modifications.

IP isn't useful if it isn't testable in the lab or on the production floor. For lab tests, Synopsys obtains split-lot samples from foundries and evaluates them using demo boards, performing eye-diagram-mask tests using bench-top oscilloscopes (**Figure 1**). For production test, Synopsys builds diagnostic IP into its PHYs—essentially on-chip sampling oscilloscopes accessible through a JTAG port, enabling a conventional digital tester to perform real-time eye-diagram-mask testing. Nandra elaborates on the on-chip test technology in **Reference 3**.

MIXED-SIGNAL FLOWS

The ultimate goal of mainstream-EDA companies is to bring what they might perceive as the pushbutton ease of operation of digital-design flows to analog- and mixed-signal design. Mixed-signal design, says Steven Lewis, product-marketing director at Cadence Design Systems, has traditionally involved forcing the analog domain within the digital domain or vice versa. Citing the comments of Intel's Rattner regarding digitally assisted analog, Lewis says that forcing one domain into another is becoming untenable. "At 65 and 45 and 32 and 22 nm, you have this blurring of lines," he says. "It's not so obvious where the analog and digital pieces begin and end."

An isolated analog/digital approach is no longer sufficient and must give way to approaches that permit top-down design and that let customers mix methodologies, according to Sandy Mehndiratta, group director for custom ICs at Cadence. Lewis adds that an effective design strategy must also support multiple geographically dispersed design teams having diverse skills.

The Cadence approach, says Lewis, is "to build an umbrella solution" that allows engineers to work in whichever domain makes the most sense for them. To that end, Cadence works to break down the boundaries between analog and digital verification as well as analog and digital implementation (**Figure 2**).

To allow each domain to understand the other without translation, the implementation stage, for instance, brings Cadence Virtuoso and Cadence Encounter together under Si2's OpenAccess, which Lewis describes as necessary but insufficient for an effective mixed-signal flow. Cadence engineers have brought Virtuoso and Encounter together, ensuring the maintenance of digital connectivity during analog editing and the locking of analog portions during digital-floorplanning adjustment. Within the combination, Encounter supports PCells (parameterized cells), multipart paths, and guard rings. Lewis says that a customer has reported a 25% reduction in overall mixed-signal-design-cycle time.

Magma based its approach on technology it obtained with the February acquisition of Sabio Labs. Magma's Hershenson, who was formerly chief executive officer of Sabio, says that the technology accelerates mixed-signal- and analog-design migration through Magma's Titan Chip Finishing and Titan Analog Migration platforms. Titan employs a unified-database architecture and supports fast shape-based routing and full-layout editing; it includes a complete encapsulation of Magma's Talus digital-design platform and Quartz DRC (design-rules-checking) and Quartz LVS (layout-versus-schematic) verification tools. Titan can also instantiate PCells.

Magma integrates the Titan Analog Migration platform with the company's FineSim, which in turn supports multi-CPU Spice simulation. Titan Analog Migration allows engineers to migrate their analog designs from one process node to another in a matter of hours, says Hershenson. Indicative of

AT A GLANCE

- Full automation of analog- and mixed-signal design remains elusive.
- Integrating the analog and the digital portions of a mixed-signal design can take weeks, and, for every process node, analog-system engineers must manually re-create designs.
- Companies making digital chips want to implement their high-speed I/O in standard deep-submicron digital processes—with all the attendant process-variation and signal-integrity issues.
- Mixed-signal design has traditionally involved forcing the analog domain within the digital domain or vice versa.

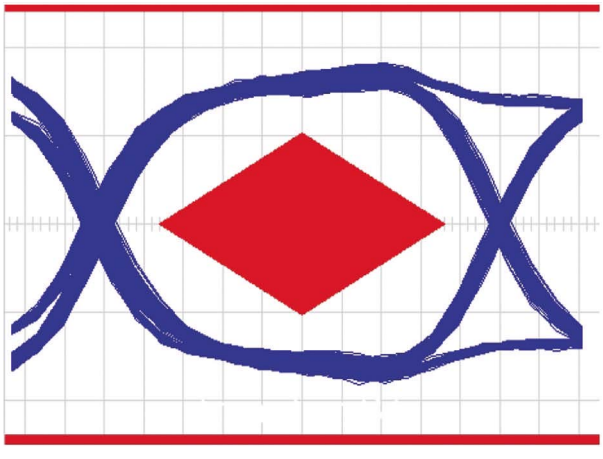

Figure 1 An eye-diagram-mask test illustrates the performance of Synopsys PHY IP for PCIe 2.0. You can directly observe the diagram on an oscilloscope from a demo board; for production test, an internal sampling-scope function makes the eye diagram available to a standard digital ATE (automatic-test-equipment) system through a JTAG port.

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Titan Chip Finishing's speed, she said it can open a 42-Gbyte file in 4 minutes and can redraw a full chip in 8 seconds.

Mentor Graphics' approach is to bring together design-implementation and -verification tools into an analog/mixed-signal-design flow that a data-management system governs (**Figure 3**), according to Min-Fang Ho, general manager of Mentor's custom-IC division. The Design Manager data-management tool allows users to collaborate among multiple sites or handle revision control. Other components include Design Architect IC for schematic capture, IC Station and ICassemble layout and assembly tools, Eldo and ADiT simulators, and Calibre physical-verification tools.

Henry Chang, Mentor's director of marketing for analog- and mixed-signal tools, elaborates on the simulation portion of the flow. Eldo is a Spice-based simulator, Eldo RF adds RF extensions, and ADiT is a fast Spice simulator that trades some accuracy for speed. Mentor's ADVance tool, he says, brings together those simulators and combines them with Mentor's ModelSim digital simulator to verify complete mixed-signal designs.

IDMs (integrated-device manufacturers) and foundries also offer mixed-signal-EDA tools. Austriamicrosystems, for example, offers the HIT-KIT (high-performance-interface-tool kit)—a utility comprising software programs and libraries that support behavioral simulation, digital synthesis, schematic capture, mixed-signal simulation, layout, design verification, and back-annotation within Cadence, Mentor, and Synopsys design environments. According to Thomas Riener, general manager of austriamicrosystems' full-service-foundry-business unit, the kits provide a consistent user interface for the company's internal designers and foundry customers. Thomas Mörth, manager of design support at the foundry-business unit, notes that the kits add custom features, such as the ability to verify that, with transistors operating at 3.3, 20, 50, and 120V on a single die, each transistor remains within its safe operating range.

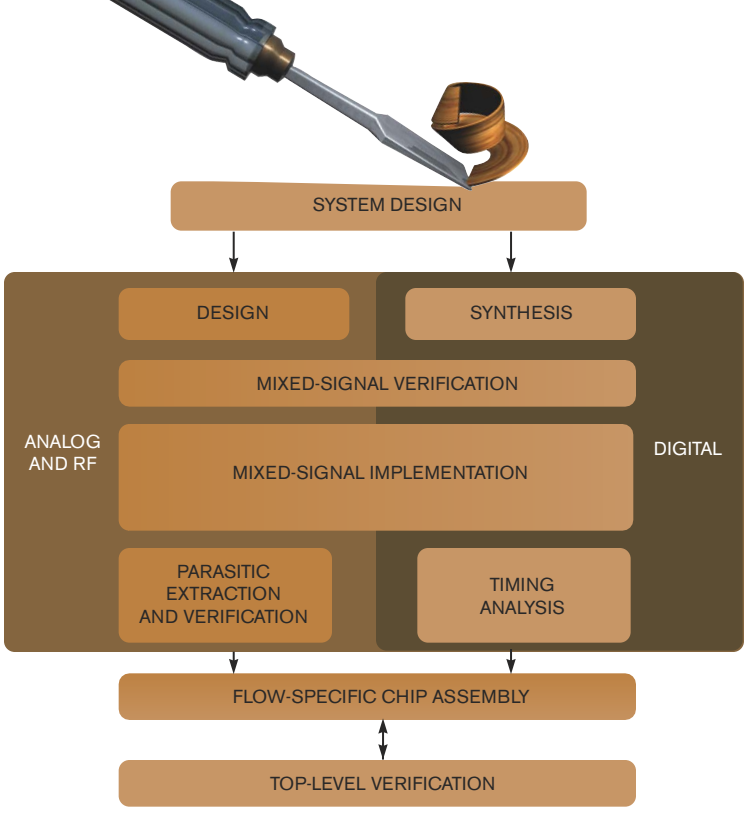

Figure 2 Breaking down the boundaries between analog and digital verification and implementation is the goal of Cadence's mixed-signal-design flow. The implementation stage, for instance, brings together Virtuoso and Encounter under OpenAccess, allowing each domain to understand the other without translation.

LOOKING TO THE FUTURE

As for what designers would like to see from EDA companies, topping the list are multithreaded versions of Spice that can take full advantage of multicore processors. Austriamicrosystems' Mörth notes that, although some Spice implementations use multiple cores, they generally rely on a single core to solve the set of matrix equations that describe the simulated circuit. "You can buy more and more hardware, but it gets to a point where that no longer helps," says Riener. "If you want to do a top-level simulation that takes three weeks, it will continue to take three weeks no matter how many CPUs you add to your server farm."

Steven Daniel, worldwide R&D manager of the analog, mixed-signal, and power division at Freescale Semiconductor, and Erwan Hemon, the worldwide automotive-IC-creation manager at the same division, also would like to see faster simulators. "Top-level simulation of a full chip with analog and digital components is a long and difficult process that can take a month at minimum and is not user-friendly," says Hemon. The process needs acceleration through parallel-processing support.

Freescale engineers employ many proprietary, in-house design-automation tools that provide leading-edge performance not available from commercial tools, but Hemon notes that a commercial tool could be a viable alternative once an internal tool has lost its ability to provide differentiation. Daniel and

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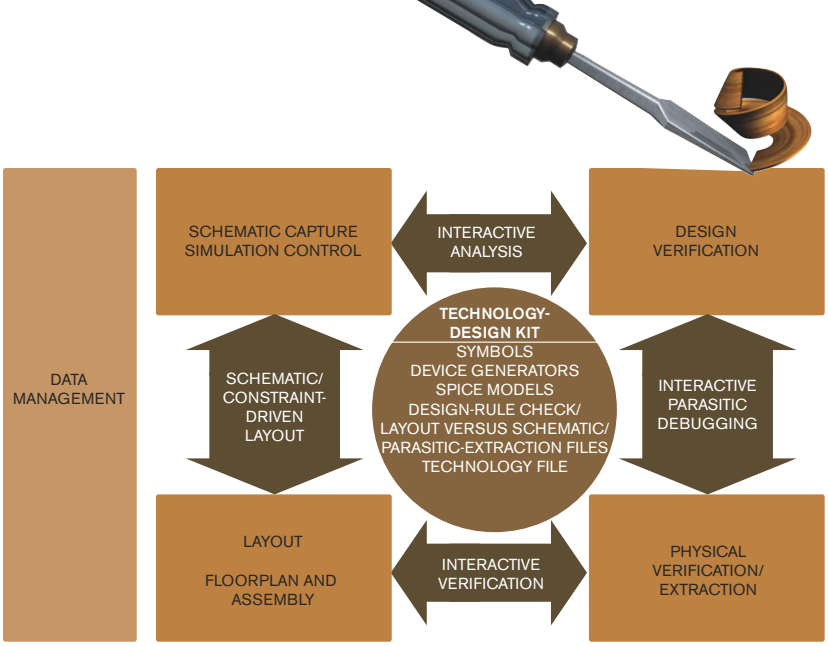

Figure 3 Allowing users to collaborate among multiple sites, Mentor Graphics' Design Manager data-management tool orchestrates an interactive analog/mixed-signal design flow. Within the flow, Design Architect IC handles schematic capture and simulation control; IC Station and ICassemble perform layout, floorplanning, and assembly; Eldo, ADiT, and ICAnalyst handle design verification; and Calibre DRC/LVS and Calibre xRC handle physical verification and extraction.

Hemon list several features they would want to see in commercial tools: support for high-voltage transistors, not just low-voltage CMOS transistors; the ability to model ESD (electrostatic-discharge) effects; and the ability to predict defect rates and aging effects. To capture defects in the analog portion of mixed-signal silicon, Hemon says Freescale engineers would like to develop a test methodology similar to the digital domain's IDDQ (integrated-circuit-quiescent-current) test. Finally, they would like to see test-program-generation support.

EDA vendors aren't specific about what's just over the horizon, but Cadence's Lewis says his company is looking at bringing assertion-based approaches—common in the digital world—to facilitate verification and test of mixed-signal designs.

Mentor's Ho says that efforts are under way to improve the communication of design intent from the schematic-capture and simulation area to the implementation area. Such an approach would invoke principles and guidelines that would facilitate automation of some tasks but still provide flexibility. Chang says that, to support mixed-signal design and implementation at 45-nm process nodes, foundries and EDA companies will need to work closely together to develop complex device models that designers can efficiently simulate. Finally, Ho notes, printability issues are affecting designs at 40 nm, and manufacturers might btter address those issues at the design stage rather than through RET (reticle-enhancement-technology) and OPC (optical-process-correction) techniques.**EDN**

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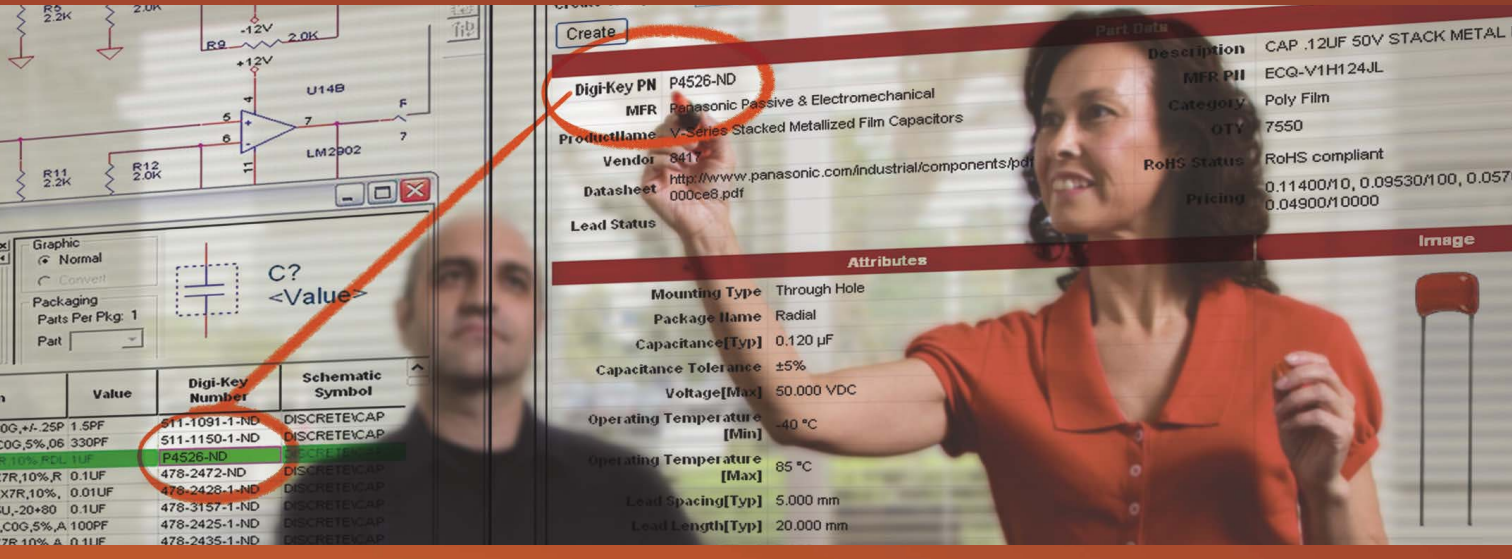

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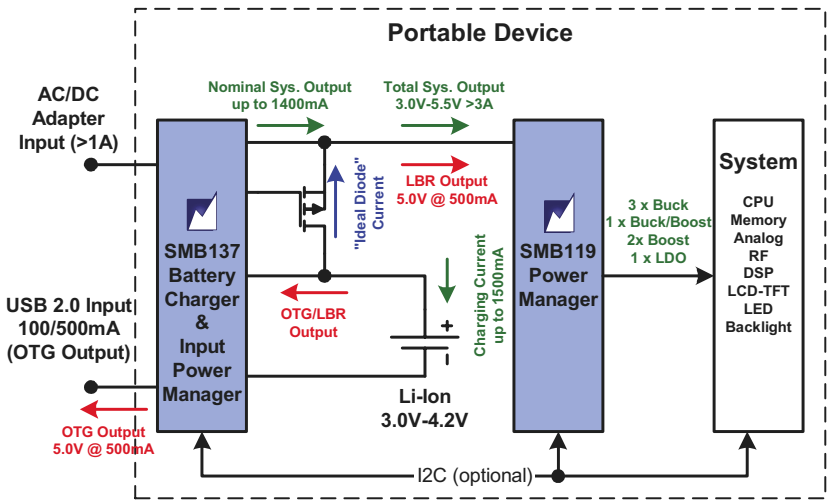

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- Handheld GPS Terminals
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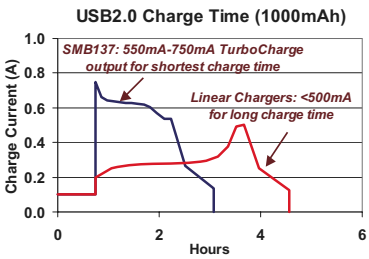

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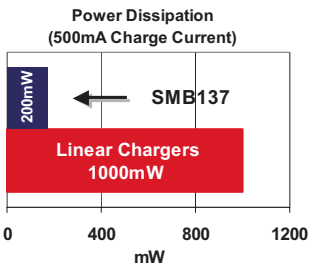
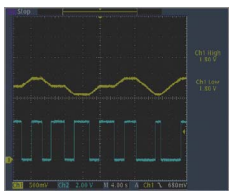


75% Lower Power



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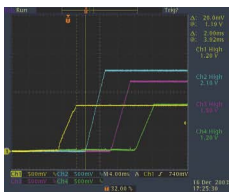

Sequencing

Programmable Battery Chargers

Product	SMB137	SMB138	SMB135/235	SMB139/239
Topology	Switch-mode	Switch-mode	Switch-mode	Linear-mode
Input Voltage Range (V)*	4.35 to 5.5 (16)	4.35 to 6.2 (16)	4.35 to 6.5 (10)	4.35 to 6.5 (10)
# of Inputs/Outputs	2/2	1/1	1/1	1/1
Maximum Charge Current (mA)	1500	1250	900	210/525
TurboCharge™ Output	Automatic	Automatic	Software/uC	
CurrentPath™ Control	X			
USB On-The-Go Power	X	X		
Low-Battery Recovery Mode	X			
I2C Interface	X	X	X	X
Programmable Algorithm	X	X	X	X
UV/OV/Thermal/Timer Safety	X	X	X	X
Package	3.6x3.3 CSP-30	3.1x2.1 CSP-20	2.1x1.3 CSP-15	2.1x1.3 CSP-8
Total Solution Size (mm2)	50	28	31	7.5

* () Indicates maximum input overvoltage "holdoff"

Programmable Power Managers

Product	SMB122	SMB119	SMB118	SMB113
Total # of Outputs	9	7	7	4
Step-down (Buck)	3 or 4	3 or 4	3 or 4	4
Step-up (Boost)	2 or 4	2 or 3	1 or 2	
Inverter (Buck-Boost)	0 or 1			
Battery Charger	1		1	
LDO	1	1	1	
Package Size (mm)	9x9	7x7	7x7	5x5

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Using FPGAs in consumer electronics

IN COST-SENSITIVE CONSUMER-ELECTRONICS PRODUCTS, CUSTOMIZATION IS A HIGHLY DESIRABLE FEATURE FOR DIFFERENTIATING YOUR PRODUCT FROM COMPETITORS' OFFERINGS. THE INCLUSION OF FPGAs CAN BE AFFORDABLE, EVEN IN LOW-RANGE AND MIDRANGE PRODUCTS, BUT STILL ALLOWS CUSTOMIZATION THROUGH SOME UNIQUE FEATURES.

It may seem odd to be reading about analog-audio and -video processing when the industry is currently focusing on the analog transmission switch-off and the digital-broadcasting successor. However, for legacy reasons and because of the increase in demand from markets that have later switch-off dates, such as East Europe, India, and South America, it is likely that analog decoding will be a requirement well into the next decade.

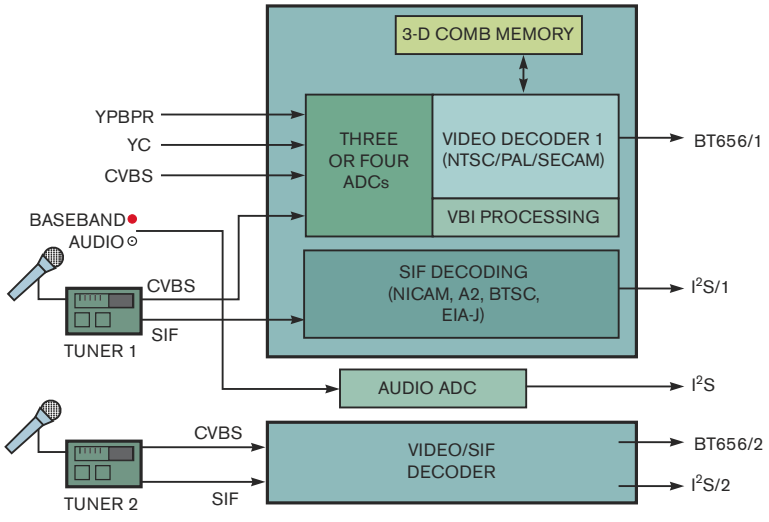
Several typical blocks constitute analog-front-end-acquisition circuits (**Figure 1**). You generally achieve the SIF (sound-intermediate frequency) and video decoding through the use of one or two ICs from a number of manufacturers. The system requires external memory if it includes a 3-D comb filter, as well as, perhaps, a baseband-audio-stereo ADC. Repetitions of these blocks exist in multituner-system configurations.

CORES VERSUS ICs

Video- and audio-decoding IP (intellectual-property) cores conceptually allow the replacement of these ICs with FPGAs. Area-efficient implementations enable you to incorporate the functions in cost-effective FPGA products, such as Altera's (www.altera.com) Cyclone and Xilinx's (www.xilinx.com) Spartan families. One way to keep down the cost of the FPGA is to allow different FPGA images for different standards, with the main control processor downloading the appropriate image depending on the detected standard. Image sets might comprise, for example, NTSC (National Television System Committee) and BTSC (Broadcast Television Systems Committee) or PAL (phase-alternating line) and NICAM (near-instantaneous companded-audio multiplexed). Using the main control processor to initialize the FPGA also offsets the cost of an EEPROM to hold the FPGA image.

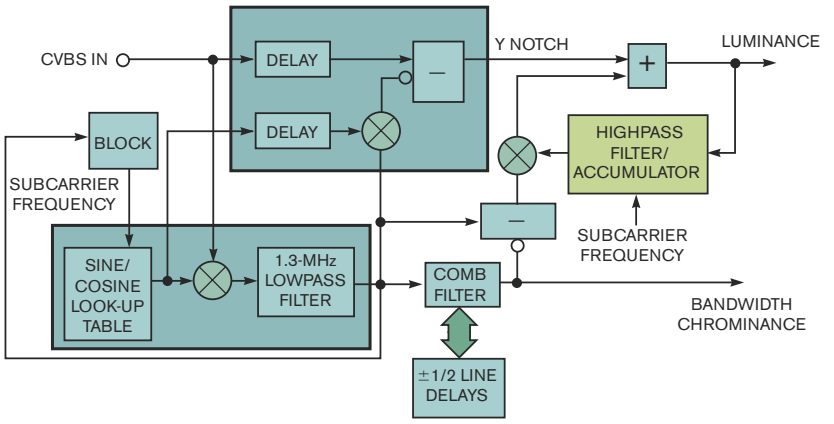
The FPGA does not incorporate significant analog functions; an external IC must perform the analog-to-digital conversion. Such ICs are available from a number of manufacturers, such as Analog Devices (www.analog.com), which offers the AD9981. The ADC also performs synchronization-separation and clock-generation functions and can interface to CVBS (composite-video-broadcast-signal), YC (S-video), YPbPr (green/blue/red), and RGB (red/green/blue) inputs. An external ADC usually achieves a better SNR (signal-to-noise ratio) than that of an integrated alternative, but the cost of implementation is about 50% higher than that of a standard-IC option. However, integrating additional functions into the FPGA can mitigate this cost increase.

For example, it is common for recorders to allow users to record one channel while watching another or for televisions to have picture-in-picture features. Such capabilities require two digital tuners, two analog tuners, two decoders, and, therefore, two sets of ICs in the non-FPGA implementa-



NOTES:
BTSC: BROADCAST TELEVISION SYSTEMS COMMITTEE.
CVBS: COMPOSITE-VIDEO-BROADCAST SIGNAL.
EIA-J: ELECTRONIC INDUSTRIES ASSOCIATION OF JAPAN.
I^2S: INTER-IC SOUND.
NICAM: NEAR-INSTANTANEOUS COMPANDED-AUDIO MULTIPLEXED.
NTSC: NATIONAL TELEVISION SYSTEM COMMITTEE.
PAL: PHASE-ALTERNATING LINE.
SECAM: SÉQUENTIEL COULEUR AVEC MÉMOIRE.
SIF: SOUND INTERMEDIATE FREQUENCY.
VBI: VERTICAL-BLANKING INTERVAL.
YC: S VIDEO.
YPBPR: GREEN/BLUE/RED.

Figure 1 Several key function blocks constitute a typical front-end-acquisition circuit.



NOTE: CVBS: COMPOSITE-VIDEO-BROADCAST SIGNAL.

Figure 2 Nontraditional comb-filter designs maximize image quality and still fit within the memory budget available in small, cost-effective FPGAs.

tion. However, you can embed two decoders within one small FPGA, thereby limiting the incremental cost to one additional ADC. To reduce area, it may be possible to limit decoder options for the secondary channel by, for example, omitting SECAM (séquentiel-couleur-avec-mémoire) decoding. The total cost of the FPGA option, as a result, will be similar to or even less than that of the IC option.

TUNER ALTERNATIVES

Next, consider how to include additional functions in the FPGA. The conventional metal-"can" analog tuner contains two main functions: an RF tuner and a demodulator. You can reduce the cost of the tuner by alternatively performing demodulation digitally within the FPGA. The video ADC can digitize the video IF. The cost savings from eliminating the need for a tuner will double in the case of dual-tuner products. This option also opens the possibility of using a silicon tuner, whose performance is now adequate for most consumer products. The silicon tuner, with its all-region capability, brings possibilities for cost-effective, all-region consumer products with corresponding manufacturing-cost savings. Metal-can tuners, conversely, are usually region-specific for unit-cost reasons.

Another FPGA-enabled possibility is to add local intelligence through the integration of a small microcontroller core for front-end functions, thereby offloading that requirement from the main controller. For example, a microcontroller can issue a simple high-level instruction to tune channels. Advantages of this approach include faster initial channel-acquisition times and the ability to power down more of the main controller under standby conditions; this approach has appeal in today's "green" society.

You can incorporate additional functions for higher-end consumer products by integrating the SDI (serial-digital-interface) receiver. FPGAs now offer LVDS (low-voltage-differential-signaling) receivers and clock-recovery circuits, which permit the implementation of an SDI receiver with just an external cable-equalizer IC. This approach is considerably cheaper than using a complete SDI-receiver IC.

IC-based video-decoder options usually also strip off the information in the vertical-blanking area of the signal, but they leave the processing of that portion of the signal for the main processor. Again, having some specialized hardware and a local controller within the FPGA permit, for example, closed-caption decoding. Decoding closed-caption or Teletext subtitles is common in televisions, but less so in PVRs (personal video recorders) and DVD (digital-video-disc) recorders. However, superimposing the subtitle on the output BT656 video, as an FPGA can do, allows the recording of subtitles for deaf and partially deaf users. You could embed the decoded subtitles in the MPEG (Mov-

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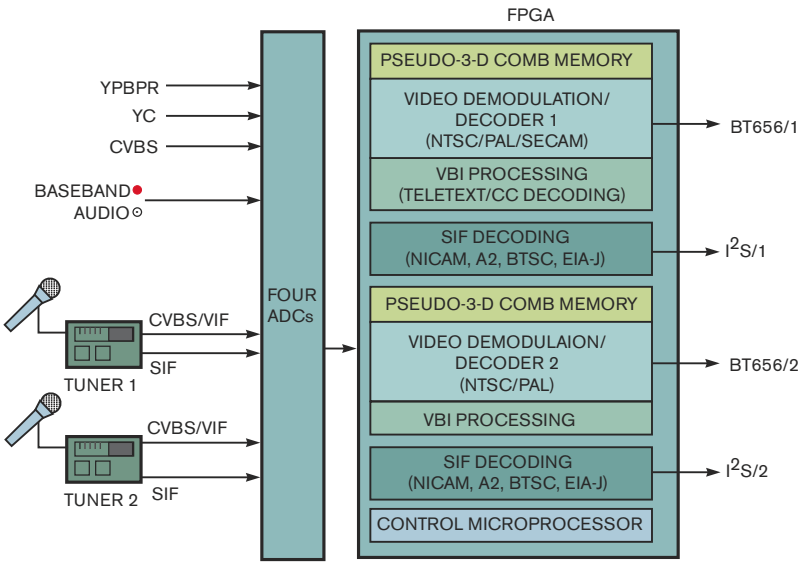

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SIF: SOUND INTERMEDIATE FREQUENCY.
VBI: VERTICAL-BLANKING INTERVAL.
VIF: VIDEO INTERFACE.
YC: S VIDEO.
YPBPR: GREEN/BLUE/RED.

Figure 3 An FPGA-based design provides for feature customization and is cost-feasible for low-end- and midrange-system configurations.

ing Picture Experts Group) metadata for a more elegant approach.

COMB IMPLEMENTATIONS

Another potentially integrated function is an improved comb filter. Most consumer products use a 2-D comb, which leaves undesirable decoding artifacts that also consume valuable bandwidth if compressed. A good 3-D comb can noticeably improve quality, but it requires an external-memory device. Available 3-D-comb-IC options use a symmetrical frame comb, which for PAL requires four frames×625 lines×1440 pixels×8 or 10 bits=36 Mbits, thereby necessitating an external-memory device, usually an SDRAM. You can halve this requirement by using an asymmetrical comb, which has the advantage of requiring no compensating audio delay. You can halve it again for PAL by using PAL modifiers in the comb architecture. An additional halving of memory budget can occur with the use of a field comb.

A single-tap, 262-line comb for NTSC or a 312-line comb for PAL gives excellent results, although it does not permit perfect decoding of complex still frames. However, for real-life images, the wide aperture of the PAL-frame comb often means that the 3-D comb will fail on moving images and thereby regress to line-comb mode. A field comb offers a good compromise between memory requirements and performance. For PAL, a field comb requires 312 lines×1440 pixels×8 bits minimum=3.6 Mbits. Unfortunately, this capacity is still too large to enable the use of integrated memory in small, cost-effective FPGAs.

However, it is possible to implement a pseudo-3-D comb that fits within the memory requirements of even the smallest FPGAs. Normally, three comb modes are available to the decoder: the 3-D comb, a 2-D line comb, and a simple mode that is either a lowpass or a notch filter. The decoder chooses the appropriate comb mode, basing its decision on signals that indicate failure conditions, such as motion, which prevents the 3-D comb from operating, or diagonals, which prevent the 2-D comb from operating. An often-assumed priority is that 3-D is always the preferred mode and that simple mode is the least desir-

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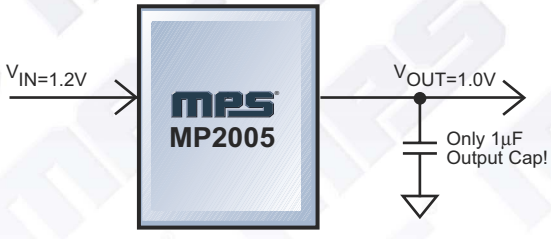

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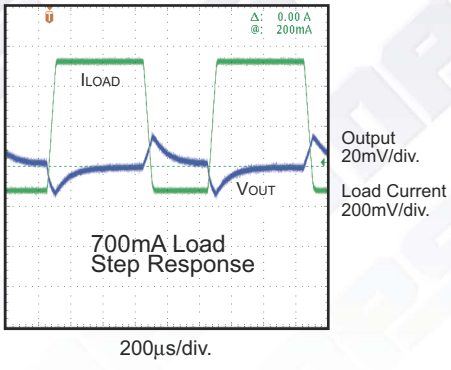

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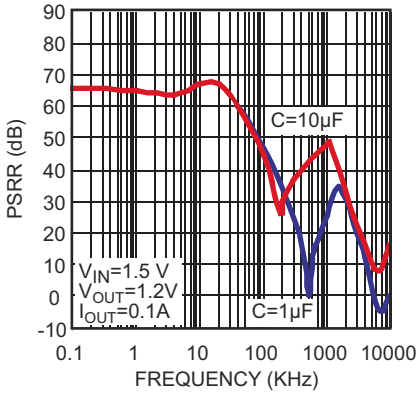

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MP8801	150mV (150mA)	150mA	2.7V - 6.5V	1.25V	Adj/Fixed	TSOT23-5
MP8802	230mV (250mA)	250mA	2.7V - 6.5V	1.25V	Adj/Fixed	TSOT23-5
MP2002	290mV (500mA)	500mA	1.35V - 6.5V	0.5V	Adj	QFN8 (2x3)
MP89046	360mV (600mA)	600mA	2.5V - 6.5V	0.5V	Adj	QFN8 (2x3)
NEW MP2005	<90mV (800mA)	800mA	1.0V - 5.5V	0.5V	Adj	QFN8 (2x3)

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able mode. However, this prioritization is not always true; on flat areas of color, for example, simple mode is often the best mode, as measured by highest SNR or least visible artifacts. The reason for this seeming disparity is that the wide aperture of the 3-D comb means that clock jitter can leave a residual subcarrier; just 1 nsec of clock jitter across an 80-msec tap distance can result in this scenario.

You can, therefore, consider a comb architecture in which the 2-D and simple modes decode an image wherever possible. Such an approach uses the 3-D comb only when neither the simple nor the 2-D modes can operate. To create this design, the system stores in memory a 1-bit positional flag along with the frame- and field-delayed data for that flag position. On the subsequent frame or field, the design can then choose a 3-D-comb aperture for these positions in addition to the 2-D and simple modes. A number of tested images, including the ubiquitous Snell and Wilcox moving-zone plate, reveal that 3-D is rarely necessary under these constraints. It is still necessary to determine whether the 3-D comb is failing. It fails, for example, if substantial motion is in the image, especially if you use a frame aperture. A considerably reduced memory requirement is the benefit, however.

A 1-bit plane is necessary for the 3-D comb aperture. For example, a 312-line field comb needs 312×720=224,640 bits. Also, at the flagged locations in which both the 2-D and the simple modes fail, the design needs memory to store the delayed information. Surprisingly, this memory budget is limited to just 32 kbytes and still produces substantial improvements in the decoded image. In other words, for a large range of images, there are just 32,000 pixels for which the 3-D comb is essential. This combined amount of memory is available even in small FPGAs, allowing the pseudo-3-D comb to operate on at least one decoder channel.

MEMORY BUDGET

A modified comb architecture yields another improvement in decoding quality. VCRs (videocassette recorders) use a color-under technique for recording. The luminance information FM-modulates onto an approximately 3.5-MHz carrier, whereas the chrominance information, along with the luminance information it contains, remodulates onto a carrier with a frequency of approximately 600 kHz to avoid problems recording at higher frequencies. Because of this remodulation of the chrominance component onto another carrier, this approach loses the phase relationship with the original subcarrier. It's therefore no longer possible to comb the higher-frequency component of the signal to separate the luminance and chrominance. The system therefore discards the higher-frequency information, resulting in a low-resolution image.

Most comb filters use a complementary-baseband comb. Composite-video demodulation occurs using a lowpass-filtered, phase-locked subcarrier waveform to produce the chrominance outputs. Combing the chrominance signals then removes the luminance components; remodulating and adding chrominance produces a clean chrominance-only signal, centering on and in phase with the subcarrier frequency. Subtracting this signal from the composite video produces clean luminance.

You can use a variant of this comb architecture, wherein the remodulation and the subtraction from the composite source occur before the comb filter (**Figure 2**). This technique produces simple chrominance components and a clean, notched luminance. Combing the chrominance components to produce combed-chrominance outputs and then subtracting them from their simple versions leaves you with the high-frequency-luminance signal. Remodulating it and adding it to the notched luminance effectively fills in the information missing from the notch. The advantage of this architecture is the ability to add the high-frequency luminance to the notched luminance using a different phase of the subcarrier. Remodulating the high-frequency luminance, the original phase relationship reconstructs the original waveform with a higher bandwidth.

You base adjustment of the phase of the second remodulator on information

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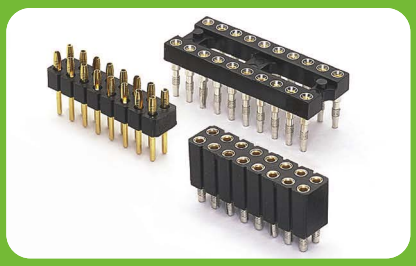

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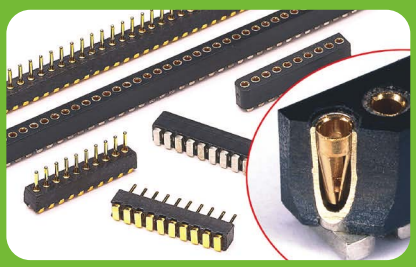

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you derive from a highpass filter. You can determine the correct phase for the addition of the luminance signals by detecting the improved sharpness of the luminance signal for particular subcarrier phases. This approach is possible using a highpass filter, a square-law function to rectify the highpass-filter output and increase the weighting to the slope of the signals, and an accumulator to measure the amount of edge detail in the image. Correct phase adjustment is an iterative process, albeit a satisfactory one because the phase changes at a slow rate. The additional phase offset adds to the subcarrier phase you derive from the input signal. This method can substantially improve the perceived sharpness of any VCR source and reduce the discrepancy between the performance of the VCR and that of the DVD. It is ideal, for example, in transcriptions.

Incorrect timing of luminance and chrominance is common with some video sources, such as VCRs. Noncoincidence of vertical edges leads to a lack of clarity in the resultant video image, specifically with regard to smearing of vertical edges. Many video decoders offer a YC-delay control, which allows the user to vary the comparative delay. However, the problem with this manual-control method is that the user needs to know the delay to be able to compensate for it, effectively rendering the control redundant. Such adjustment is difficult to do visually, especially for an unskilled user, and it requires specific video-test patterns to properly perform the adjustment. The delay can also vary over time, especially for mechanical mechanisms, such as VCRs. However, the FPGA can incorporate methods not available in off-the-shelf IC decoders to automatically, periodically retime the luminance and chrominance.

AUDIO APPROACHES

Audio acceptance occurs in either an SIF (sound-intermediate frequency) from the tuner, such as NICAM or BTSC, or baseband stereo from the composite- or component-video inputs. ICs demodulate and decode the SIF signal; similarly, IP cores that perform these functions are available for FPGAs. As mentioned, the FPGA can take advantage of different configurations for different standards to reduce the area impact, and it can incorporate additional decoders for multituner products.

IC options may integrate the baseband-audio ADC with the video decoder. However, this approach usually results in a worse SNR than that of an external-IC alternative. However, it is possible to also use one of the video ADCs for the audio. By substantially oversampling the audio and then decimating the result, you can theoretically achieve the additional needed bits without using an external device, leading to further cost savings (**Figure 3**).EDN

AUTHOR'S BIOGRAPHY

Phuttachad Thiencharoenwong is sales director for SingMai Electronics. Before emigrating to Canada, she ran her own civil-engineering company, ODP Engineering, in Thailand and Singapore and previously sold electronic components in Thailand.

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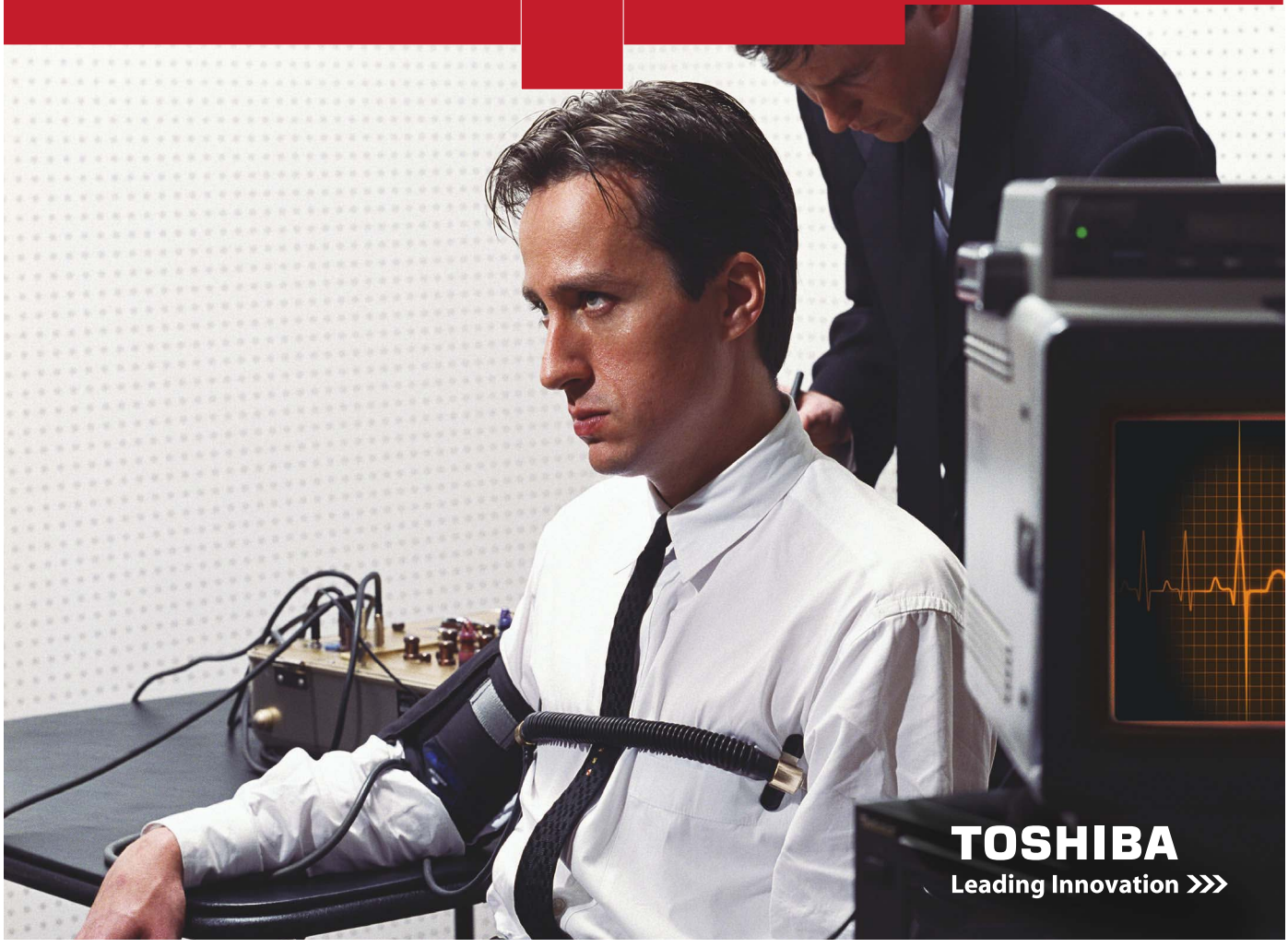

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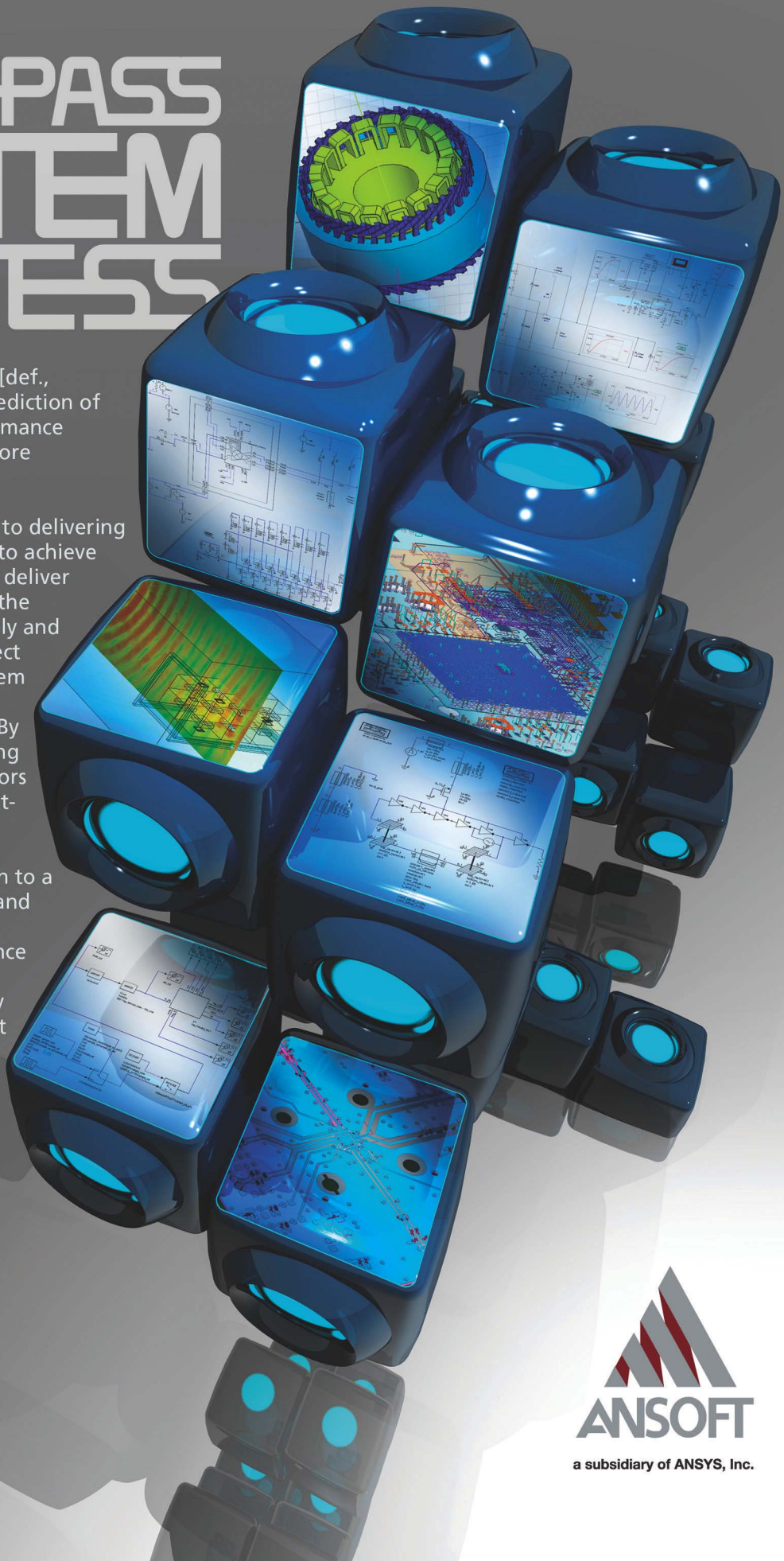

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BY DAVID LAUTZENHEISER AND AGHA HUSSAIN • SILISTIX

Optimize memory-system design for multimedia applications

THE CONVERGENCE OF VIDEO AND COMMUNICATIONS IN INEXPENSIVE UNIFIED-MEMORY ARCHITECTURES HAS MADE DRAM THE MOST IMPORTANT AND THE HIGHEST-PERFORMANCE TARGET IN ANY SYSTEM.

DRAM efficiency has become a severe challenge for video-processing-SOC (system-on-chip) designers. This evolution is the result of many factors. Continued advances in process technology have enabled higher integration levels. Dominant consumer-pricing pressures have replaced higher-margin communications infrastructure and high-end computing as the market drivers. In the consumer markets, the adoption of much-higher-bandwidth-consuming standards, such as HD (high-definition) video, in consumer equipment has created enormous bandwidth requirements. At the same time, however, low-cost chip-to-chip bandwidth generally lags behind the on-chip speed increases that on-chip process technology and architectural advances enable.

All of these pressures eventually focus on the SOC-to-DRAM interface. With the convergence of video and communications in inexpensive unified-memory architectures, DRAM has become the most important and the highest-performance target in any system.

As SOCs have integrated more functions on a single chip, the additional cost along with the loss of digital-logic performance associated with integrating DRAM on that chip has forced consumer-multimedia-device manufacturers to employ DRAM as one or more separate chips. As this trend continues, it highlights the cost of the DRAM as a major component of overall system cost. To minimize system cost for a given performance level, efficient use of DRAM becomes critical. If, through intelligent SOC design, a system can use slower and therefore lower-cost DRAM or fewer DRAM devices, then that system can significantly increase its performance-to-cost figure of merit. Consequently, in recent years, DRAM-access performance and use have pushed past 50% to more than 80% in consumer digital devices.

MAXIMIZING DRAM EFFICIENCY

You can increase DRAM efficiency, but only by considering a number of complex interactions in the overall system design. Key among these interactions are communication with and the information that flows between the various system functions that use DRAM, as well as interactions with the controller logic that manages DRAM operation.

Figure 1 shows how the key processing functions that supply and manipulate DRAM data communicate with the DRAM controller. In traditional SOCs, this communications network is usually a hierarchy of clock-based, processor-oriented buses. In more modern SOC architectures, the interconnect is a separate system for managing traffic, using architectures such as a synchronous-star crossbar, clock-based NOC (network on chip) or a clockless, asynchronous NOC.

High DRAM efficiency is important for multimedia processing, particularly for devices that process HD data streams. A number of factors affect the efficiency of this processing. Though these factors vary from system to system, you need to carefully consider them when developing the architecture of a multimedia system.

The DRAM controller needs maximum visibility of the IP (intellectual-property) core making a request. The controller cannot always infer the needed information from the request: The system must explicitly communicate the information to the controller, allowing the controller to determine the importance of the new request relative to other requests already under way.

In older bus-based systems, differentiation among potential requesters was not part of the request. The controller had to infer it by some other means. For example, in AHB (advanced-

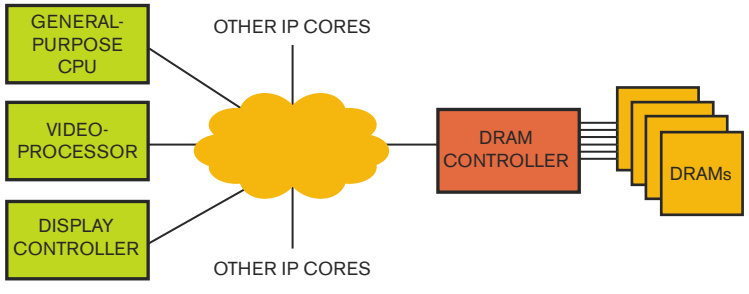

Figure 1 Key functions in a video-processing SOC include various processor and controller cores, including the DRAM controller for external memory.

high-performance-bus)-based systems, multiple AHBs allow the controller to properly weigh one request against another. These multilayer systems can use various QOS (quality-of-service) algorithms at the DRAM controller to extract the highest efficiency from the DRAM channel and still satisfy the needs of the system.

In more modern protocols, such as OCP (Open Core Protocol) or AXI (Advanced Extensible Interface), various fields in the request packet identify the requester and, potentially, the specific task from the requester, using OCP tags or AXI identifiers. Tags let the on-chip communications and its targets reorder responses to nonconflicting memory addresses within a single thread, ensuring that the system respects write ordering. Tagged transactions are useful for advanced CPU architectures. To maximize DRAM efficiency, the interconnect between requester and DRAM controller must convey all possible information about the request.

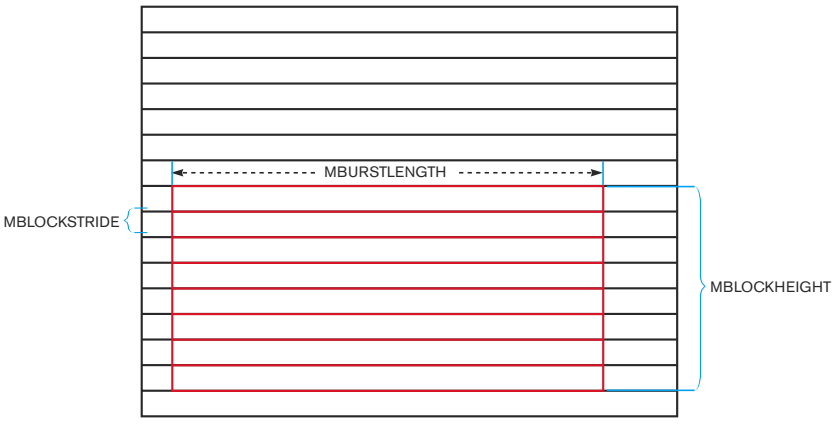

Figure 2 A 2-D block-transfer command has, along with the data comprising multiple same-length lines, information about the number of lines in the block and the offset between adjacent lines.

Modern DRAM controllers have command queues that hold outstanding requests from the multiple initiators a system might contain. To ensure that the controller has maximum flexibility in selecting command sequences and other important information, the controller queue should always contain multiple requests from which to make the best scheduling decision. For the on-chip network, there should be no barriers to delivering all possible requests as soon as possible, again with the maximum information about the requests.

One way to manage system traffic is to add traffic-shaping and traffic-ordering logic to the interconnect in front of the DRAM controller to assist the controller in DRAM management. However, as only the DRAM controller knows the state of the DRAM devices and pending requests from other system functions, request scheduling should be the job of the DRAM subsystem. Any attempt to reorder or tailor requests in any way can confuse the DRAM controller. A request that arrives early and that the system does not recognize as a priority request wastes storage. If the system recognizes it as a priority request, then it may disturb the scheduling and reduce DRAM efficiency. The network should be invisible to the DRAM and deliver requests as quickly as possible.

The best approach is to deliver the raw state of the system without overwhelming the DRAM controller, so there is a single point of resolution between the state of the DRAM devices and the needs of the system. Any other approach may introduce an opportunity for losing information or for parts of the system to make the wrong decisions, both of which reduce DRAM efficiency.

In some systems, the interconnect may modify the nature of the request such that when it arrives at the DRAM controller, it is late for an opportune scheduling window, or it may lose or subvert some aspect of the request. For example, in some time-multiplexed systems, the nature of the alloca-

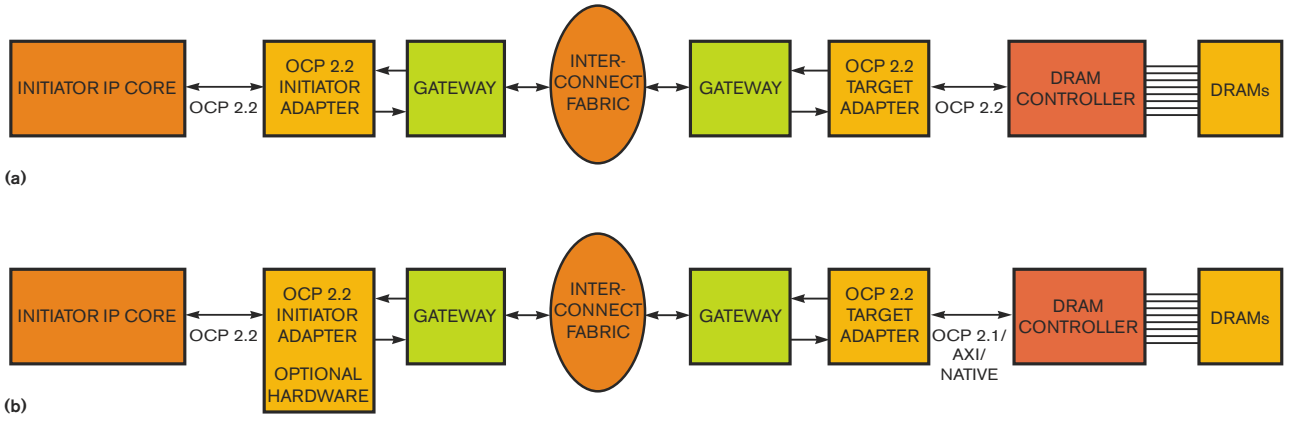

Figure 3 A 2-D block transfer using a synthesized self-timed interconnect fabric may pack MBurstSeq into IP and deliver it to a target adapter (a) or convert MBurstSeq into multiple burst requests in optional hardware at the initiator adapter (b).

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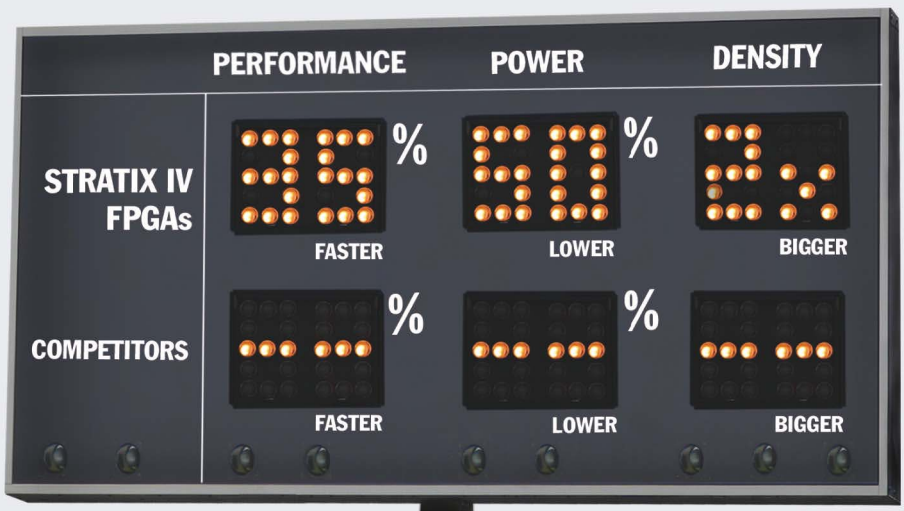

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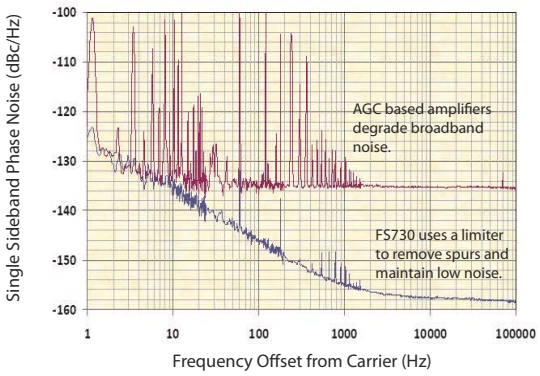

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tion algorithms causes a large transfer to break into a series of smaller transfers. At any point in servicing one of the smaller requests, the DRAM controller could have an opportunity to manipulate the DRAM controls to achieve additional efficiency if it knew that another, similar request was coming. Without that insight, the DRAM controller might close a bank or allow an intervening read to reverse the bus state, reducing efficiency.

For many DRAM controllers, the ability to reorder memory-access requests, even from a single requester, is critical for efficient operation. For maximum efficiency, the SOC architecture must incorporate some mechanism at the target that allows for this reordering across initiators, even if the requesting IP core does not support it.

TABLE 1 GUIDELINES FOR MAXIMIZING DRAM EFFICIENCY

What you need to maximize DRAM-controller efficiency	Desired attributes of synthesized-communication networks
Maximum visibility to requesting intellectual-property core needs	Interconnect carries source identification and priority if desired
Controller has a large number of requests from which to choose	Bandwidth of interconnect is typically much greater than endpoint capability
Single point of system to match state of DRAM to system needs	Interconnect is completely "endpoint-transparent"
Interconnect does not modify information	Initiator request is delivered unaltered
Requests can be reordered	Adapters have a reordering capability for endpoints that lack it

ADDRESSING DRAM-EFFICIENCY ISSUES

One way to deal with the need to fully inform the DRAM controller is to synthesize, either through a formal manual process or using an automated tool, an interconnect structure you base on the requirements of the individual requester blocks. In this instance, think of synthesis in the general sense as a translation from one level of abstraction to another and not in the specific sense as producing a gate-level netlist from an RTL (register-transfer-level) description. Such an automated tool may synthesize self-timed interconnect networks from a high-level, architectural description with several attributes that help optimize DRAM operation.

Interconnect synthesized in this way can inherently carry the identification of the requesting IP core, even if the protocol at the requesting end does not explicitly support such identification. For example, an AHB initiator, which does not have an explicit identification capability, may receive an SID (source identification) during interconnect synthesis. The interconnect carries this SID from the AHB initiator to the DRAM controller, and the controller can then use the SID in its algorithms to maximize efficiency. For protocols such as those that have explicit identification fields, the system may carry the ID information intact to the DRAM

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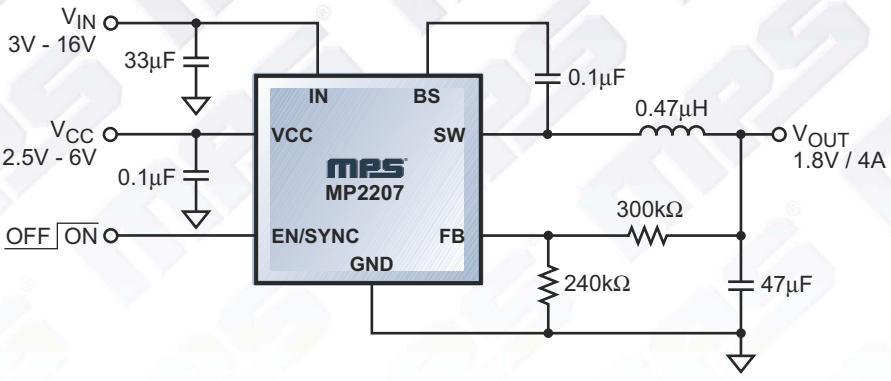

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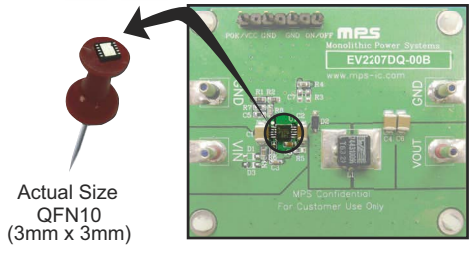

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MP28128	1.5MHz	95% @ 1.5A	60mΩ	2.7 - 6.0	0.8 - 0.9 x VIN	2.5	QFN10 (3x3)

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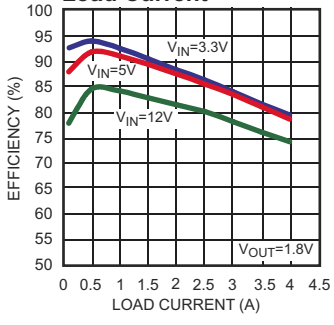
MP4460	4MHz (Adj.)	4.5 - 40 (Max)	0.8 - 36	2.5	QFN10 (3x3)
MP2467	500KHz (Fixed)	6 - 40 (Max)	0.8 - 30	2.5	SOIC8E
MP4461	4MHz (Adj.)	4.5 - 40 (Max)	0.8 - 36	3.5	QFN10 (3x3)

Efficiency vs Load Current



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controller. If the system architect wishes to include additional system-level priority or similar information about the requester, the interconnect-synthesis process may provide optional fields for this information. This situation is more desirable than dealing with buses that require the chip designer to translate all information into a form that the bus protocol can understand.

If the synthesis creates self-timed communications networks, the bandwidth of these structures is generally much greater than that of the DRAM controller. In addition, because of the nature of the aggregation that might occur in the path to DRAM, such a system can deliver all possible incoming requests bound for DRAM at maximum wire speed. This method ensures that any request arrives at the DRAM controller as soon as possible and is not, for example, caught in the interconnect waiting for a clock edge.

In general, requests to the interconnect should be completely contiguous. The system should deliver a long, unmodified request from an initiator to the DRAM controller in whatever form it began. The interconnect should not modify any of the information.

In some cases, the initiator, rather than the interconnect, should modify requests. For example, the system designer may choose to incorporate burst chopping during a write request to avoid blocking or eliminate the need for large buffers to absorb a large data burst at the DRAM controller. Such a modification to the request stream needs to happen at the initiator to match the burst sizes the target DRAM can handle. In this approach, however, the interconnect should not be a factor in the burst-chopping decision and should carry whatever request the initiator sends.

Along with the communications network, the synthesis process should also generate adapters—logic that services the needs of endpoints—with optional reordering capability. This approach allows a mixed system, such as one with both AHB and OCP initiators, to fully support reordering, allowing the

TABLE 2 IMPLEMENTATION TRADE-OFFS BETWEEN THE TWO TYPES OF MBURSTSEQ=BLCK COMMAND TRANSFERS

Implementation A		Implementation B	
Pros	**Cons**	**Pros**	**Cons**
DRAM controller has maximum command information	A limited set of DRAM controllers support MBurstSeq=BLCK	Works with a wider set of DRAM controllers	Larger area for initiator adapter
Better use of interconnect; less overhead of multiple burst commands	Initiator adapter must have more intelligence and must support a wider set of target adapters	Easier to construct systems with mixed endpoints	Overhead of multiple burst requests over interconnect; DRAM controller is "missing" information about the request

DRAM controller to operate as efficiently as possible. For an endpoint, such as one that uses AHB, a reordering adapter manages the order of requests, making them appear to the endpoint as always in order, even if the DRAM controller, for efficient operation, chooses to reorder particular requests.

Table 1 summarizes these DRAM-efficiency issues and how interconnect synthesized by a formal process can addresses them.

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A 2-D BLOCK TRANSFER

An example of a function that can improve DRAM efficiency is a 2-D block transfer. This transfer is a special form of an SRMD (single-request-multiple-data) command that passes across an interface from an initiator, through the interconnect, to a receiving target. With respect to OCP, the only publicly available protocol that currently supports this capability, the 2-D block transfer is a special burst type, MBurstSeq=BLCK.

In addition to the starting address and length (in the case of 2-D, the length of each line), this 2-D transfer request transmits a height (the number of lines in the block) and a stride (the offset from the beginning of one line to the beginning of the next) at the same time. **Figure 2** shows the structure of a 2-D block transfer as the OCP 2.2 protocol defines it.

At the receiving end—typically the DRAM controller but possibly a video display in a write-only video-processing system—special hardware stores the additional information for the 2-D burst request, manages the incrementing movement from one line to the next based on the stride, and determines the end of the burst based on the height.

Figure 3 shows two implementations of a 2-D block transfer that are receiving support from a self-timed interconnect fabric of the type synthesized by Silistix tools. Each implementation shows a single path, from the initiator to the DRAM controller; however, the initiator needs to access other paths in the system, including, possibly, other endpoints.

In **Figure 3a**, the key system flow is between an OCP 2.2-capable initiator that can issue an MBurstSeq=BLCK command and a similarly OCP 2.2-compliant DRAM controller that can directly accept the MBurstSeq=BLCK command. Thus, the DRAM controller has the registers and logic to store and manipulate the burst for its stride and height. In this implementation, the adapters at each of the critical endpoints would need to be OCP 2.2-compatible.

When it receives the MBurstSeq=BLCK burst type, the initiator adapter packs that request into the internal format that the synthesized interconnect uses and delivers it intact with the additional fields to the target adapter. The target adapter unpacks the information from the internal format and supplies it across the OCP 2.2 interface exactly as the initiator adapter received it. As the DRAM controller supplies data, the target adapter associates that data with that request and delivers it back to service the command.

In **Figure 3b**, the same OCP 2.2-capable initiator makes the request, but there is no OCP 2.2-capable DRAM controller. The DRAM controller in this case might have an AXI interface or an older OCP-compliant interface that does not support the MBurstSeq=BLCK burst type. The controller might also be a customer-specific core that uses a native interface instead of a standard protocol. In either case, the operation of the implemented circuitry is the same.

When the initiator adapter receives an OCP 2.2 MBurstSeq=BLCK burst type, the adapter determines that the target is not OCP 2.2-capable and stores the stride and height information in additional hardware. The system architect would specify this hardware during interconnect synthesis, based on a desire to support the OCP 2.2 MBurstSeq=BLCK burst type for the initiator despite not having an OCP 2.2-compliant DRAM controller. The initiator adapter would decompose the 2-D block transfer into the proper number of conventional burst transfers and begin issuing them across the interconnect to the DRAM controller. If the DRAM controller uses a nonstandard interface, the interconnect can alert the DRAM controller that multiple burst requests of this type are inbound. The system could also unroll 2-D bursts at the target and automatically deliver them to the endpoint DRAM controller, which has the same effect. Depending on the algorithms the controller uses, this information alone may improve the efficiency of servicing an MBurstSeq=BLCK type of burst.

For systems in which the OCP 2.2-capable initiator needs to issue 2-D block transfers to both OCP 2.2-compatible and non-OCP 2.2-compatible endpoints, the same options apply. The initiator adapter should be able to identify, from the nature of the request and its knowledge of the endpoint types,

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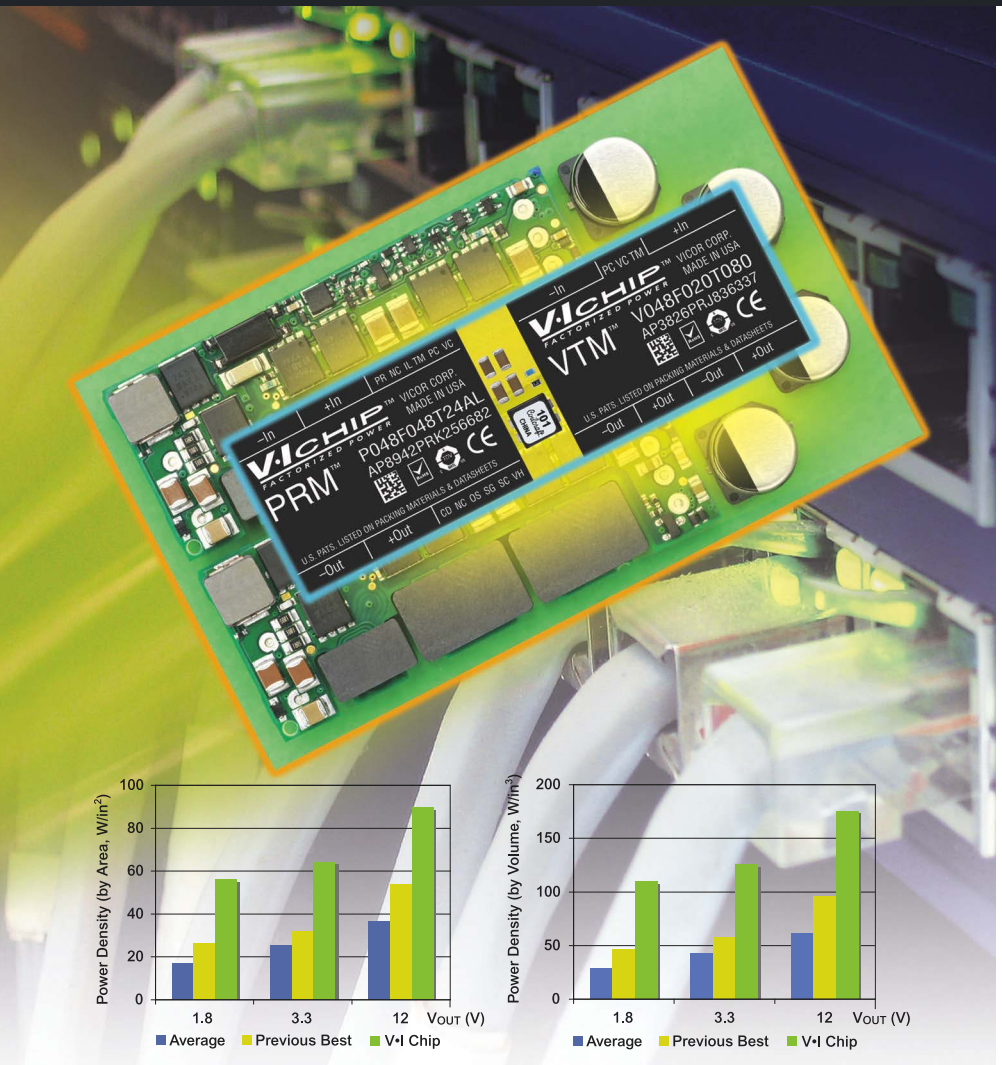

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which endpoints can directly accept the 2-D block command and which ones must use the optional hardware. This approach involves slightly more hardware overhead to service both types with OCP 2.2 MBurstSeq=BLCK burst types but allows efficient management of mixed systems.

Design teams must consider various trade-offs when evaluating the two implementations. **Table 2** shows these trade-offs relative to the two 2-D block transfer in **Figure 3**.

For either option, it is important to model the traffic interactions relative to the DRAM controller in a more abstract form. The Silistix tools can generate an OSCI- or CoWare-compatible SystemC model of the synthesized interconnect and a timed or an untimed version of the model for early system verification.

Using 2-D block transfers improves both DRAM and network efficiency; it improves network efficiency by aiding traffic flow on the network. These types of transfers improve the efficiency of both synchronous and asynchronous, self-timed networks but are particularly beneficial for the asynchronous variety. It is possible, by examining the kinds of transfers the blocks in an SOC require, to synthesize a network that can enable a DRAM controller to most efficiently mediate between the needs of the blocks and the behavior of DRAM chips. It can happen nearly independently of the individual characteristics of the blocks and the controller, as long as the architecture respects the separation between the processing and the transport functions. EDN

AUTHORS' BIOGRAPHIES

David Lautzenheiser is the vice president of marketing at Silistix. Before joining Silistix, he was in private practice, assisting innovative small companies with company and product-strategy issues and planning and executing company and product launches. Previously, Lautzenheiser successfully launched new companies and products as vice president of marketing at both Sonics and LightSpeed Semiconductor. Lautzenheiser began his marketing career at Xilinx, where he led the introduction of the first FPGAs. He holds a bachelor's degree in electrical engineering from Washington University (St Louis).

Agha Hussain recently joined Silistix as the company's chief system architect. Previously, he was an application architect at Sonics, working in the digital-media and wireless areas for applications such as DVD, DTV, cell phones, and WiMax. In addition, he was a co-founder and vice president of hardware platforms for Network Utilities and worked in a variety of roles at Integrated Device Technology. His interests and experience include synthesis, timing and performance analysis, chip interconnect, DDR memory, and silicon-bus protocols. Hussain has a bachelor's degree from Nardirshaw Edulji Dinshaw University of Engineering and Technology (Karachi, Pakistan) and a master's degree in engineering from the University of Southern California (Los Angeles).

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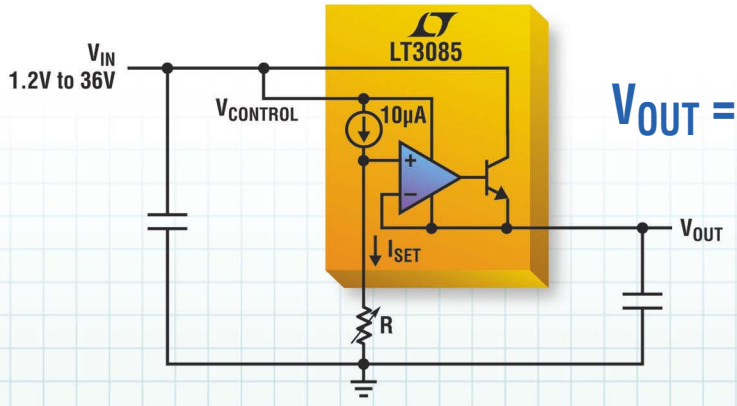

$V_{OUT} = I_{SET} \times R$

- Outputs May Be Paralleled for Higher Current and Heat Spreading
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LT308x Family

Part No.	I_{OUT}	Package
LT3080/-1	1.1A	MSOP-8E, 3x3 DFN-8, TO-220, SOT-223-3
LT3085	500mA	MSOP-8E, 2x3 DFN-6
LT3082*	200mA	3x3 DFN-8, SOT23-8, SOT-223

*Future Product. Contact Linear Technology Marketing for more information.

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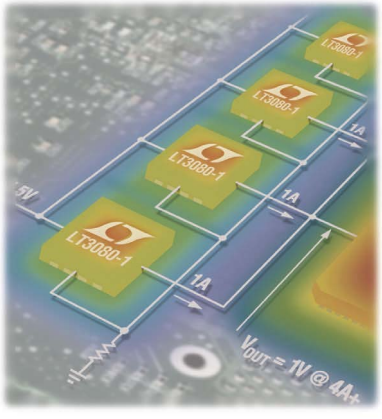

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READERS SOLVE DESIGN PROBLEMS

Platinum-RTD-based circuit provides high performance with few components

Jordan Dimitrov, Toronto, ON, Canada

The standard way of using an RTD (resistance-temperature-detector) sensor is to include it in a bridge followed by a differential amplifier. The problem is that two nonlinearities—one from the sensor and another from the bridge—affect the transfer function. Some approaches are available that attempt to avoid the problem, but they tend to be bulky and expensive (**references 1**, **2**, and **3**). An alternative circuit proposes adding only one extra resistor to the differential amplifier but provides neither design guidelines nor results (**Reference 4**). This Design Idea fills the gap. Although circuit analysis is somewhat complex, performance is good, and the circuit uses few components.

Besides the platinum RTD, R_Θ, the circuit features only six precision resistors, an op amp, and a voltage reference (**Figure 1**). R_4, the extra resistor for the differential amplifier, delivers additional current to the sensor that relates to the temperature you are measuring. With proper design, the circuit can provide good linearity and stability over a wide range of input temperatures. The output voltage, V_O, depends on circuit components in the following way:

$$V_O = V_{REF} \times \frac{Y_1}{Y_2} \times \frac{R_\Theta(Y_0 + Y_2 - Y_3 - Y_4) - 1}{R_\Theta[Y_1 + Y_3 - R_2 Y_4(Y_0 + Y_1)] + 1},$$

where $Y_I = 1/R_I$ and I=0 to 4.

For positive temperatures, a second-degree polynomial of the following form can approximate RTD characteristics:

$$R_\Theta = R_0(1 + \alpha \times \Theta + \beta \times \Theta^2),$$

where R_0 is sensor resistance at 0°C, α and β are coefficients, and Θ is the measured temperature.

After replacing the second **equation** in the first and doing some rearrangements, you get:

$$V_0 = \frac{\Theta - B}{\Theta^2 - B\Theta - C} \times K \times \Theta = f(\Theta)K\Theta,$$

where B, C, and K are constants and f(Θ) is a function of temperature. **Figure 2** shows the general shape of f(Θ). The output voltage depends linearly on temperature when f(Θ) is as close as possible to a constant. This situation is most true around the minimum point of f(Θ).

Some additional relations provide that the output voltage is 0V at temperature 0°C, the conversion coefficient is 10 mV/°C, the minimum of function f(Θ) is in the middle of the measurement span, and

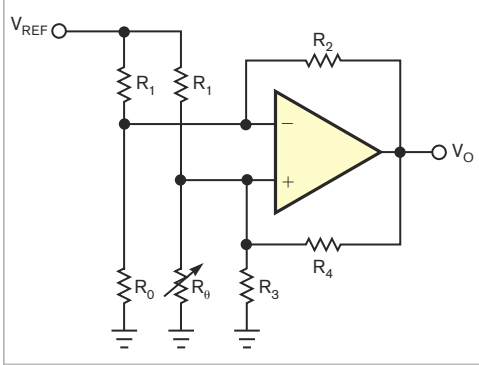

Figure 1 This generic RTD circuit needs few components.

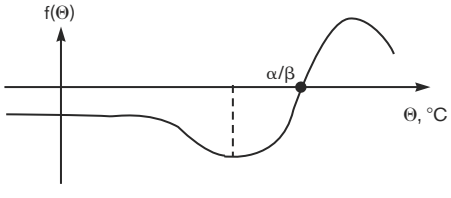

Figure 2 The general shape of function f(Θ) varies with temperature.

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the current through R_θ causes negligible self-heating of the sensor.

Figure 3 shows the circuit that meets these requirements. The sensor is a DIN-IEC 751 platinum RTD. Microsoft (www.microsoft.com) Excel software fits 13 points of 0 to 600°C in steps of 50° from the RTD's calibration table. The spreadsheet software determined R_0 to have a value of 100Ω, α to have a value of $3.908\times10^{-3}°C^{-1}$, and β to have a value of $-5.801\times10^{-7}°C^{-2}$ with an R^2 factor of one.

All the circuit's resistors have tolerances of 0.02%, and the temperature coefficient is 50 ppm/°C. You can use two trimming potentiometers, V_{R1} and V_{R2}, to independently adjust zero and span readings. You should perform span adjustment at 550°C to match the magnitudes of the positive and the negative errors. You can also extend the temperature range to start from −100°C instead of 0°C without exceeding the basic nonlinearity. The three-lead connection to the sensor significantly reduces the influence of connection-cable resistance, R_C, on accuracy.

Table 1 shows the results of evaluating this circuit's performance with a calibrated, precision-decade resistance and a calibrated, 4.5-digit multimeter with readings at ambient temperatures of 24 and 68°C; power supplies of ±12, ±15, and ±18V; and cable resistances of 0 and 5Ω. EDN

TABLE 1 EXPERIMENTAL RESULTS

Measurement range	−100 to +600°C
Nominal sensitivity	10 mV/°C
Basic accuracy (nonlinearity)	Well below ±1°C
Ambient-temperature effect	0.05°C/10°C
Power-supply effect	0.1°C/V
Cable effect (three-lead connection)	0.7°C/Ω
Power-supply range	±12 to ±18V
Consumption (600°C input)	9 and −3 mA
Operating temperature	−40 to +85°C

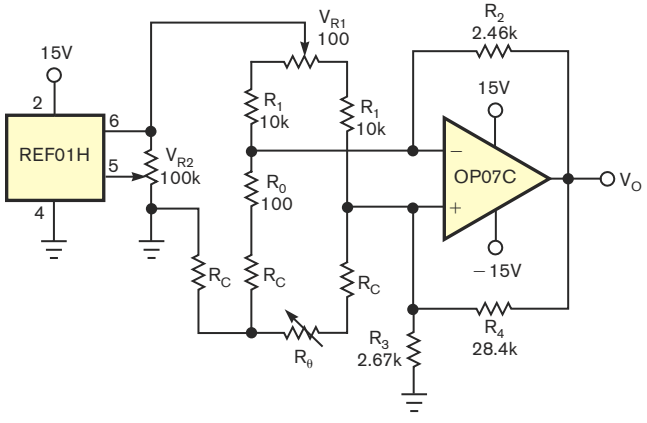

Figure 3 The full circuit needs trimming potentiometers V_{R1} and V_{R2} to adjust zero and span, respectively, and a three-lead cable for sensor connection. R_C is the cable's resistance.

REFERENCES

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3. Moghimi, Riza, "Low-error platinum RTD circuit has shutdown capability," *EDN*, Sept 14, 2000, pg 186, www.edn.com/article/CA47186.
4. Gutnikov, VS, *Integrated Electronics in Measuring Devices*, Leningrad, 1980.

Proportional-ac-power controller doles out whole cycles of ac line

Richard Rice, Oconomowoc, WI

In industrial and process control, it is often necessary to accurately control the temperature of a process. You control most heating elements using the "bang-bang" method—turning the power to them on and off at a predetermined setpoint. The temperature of the heated substance constantly hunts back and forth around the setpoint. You can achieve much greater temperature precision using proportional power control. With this method, the controller monitors the temperature, proportionally varying the heater power to keep the temperature as close as possible to the setpoint. A PID (proportional-integral-derivative) control loop usually accomplishes this function. Varying the ac power to the heating element in a linear-proportional manner is neither easy nor simple.

This Design Idea borrows from the delta-sigma-modulator concept. The controller sends cycles of the ac line to the load as the delta-sigma modulator determines. For example, when the input-control voltage is 15% of full-scale, only 15 of 100 ac cycles arrive at the load. Likewise, at 85%, 85 of 100 arrive (**Figure 1**). The control-voltage-input stage, IC_{1A}, is an inverting amplifier with a gain of negative one. This stage makes the control-voltage range over the positive side of 0V. In this example, the control-voltage input ranges from 0 to 2V full-scale. The control

DESIGN NOTES

Triple LED Driver in 4mm × 5mm QFN Supports LCD Backlights in Buck, Boost or Buck-Boost Modes and Delivers 3000:1 PWM Dimming Ratio

Design Note 449

Hua (Walker) Bai

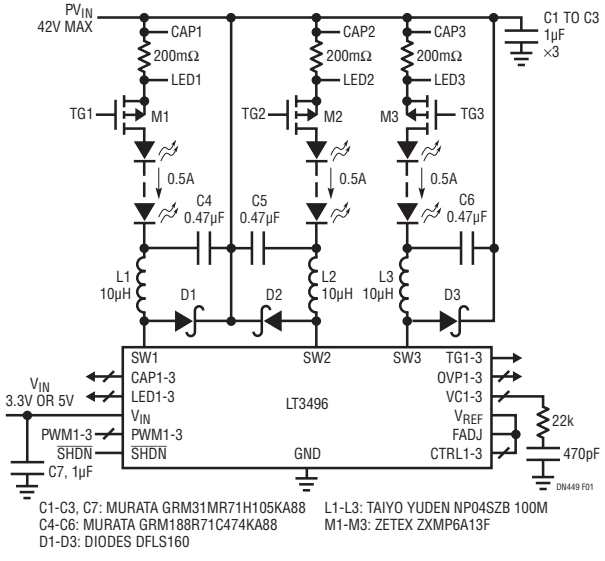
Introduction

By integrating three independent LED drivers, the LT®3496 offers a highly efficient, compact and cost-effective solution to drive multiple LED strings. All three drivers have independent on/off and PWM dimming control, and can drive different numbers or types of LEDs. High side current sensing and built-in gate drivers for PMOS LED disconnect allow the LT3496 to operate in buck, boost, SEPIC or buck-boost modes with up to 3000:1 True Color PWM™ dimming ratio.

The LT3496 is offered in a single 4mm × 5mm QFN or FE28 package. The efficiency of each driver can exceed 95%.

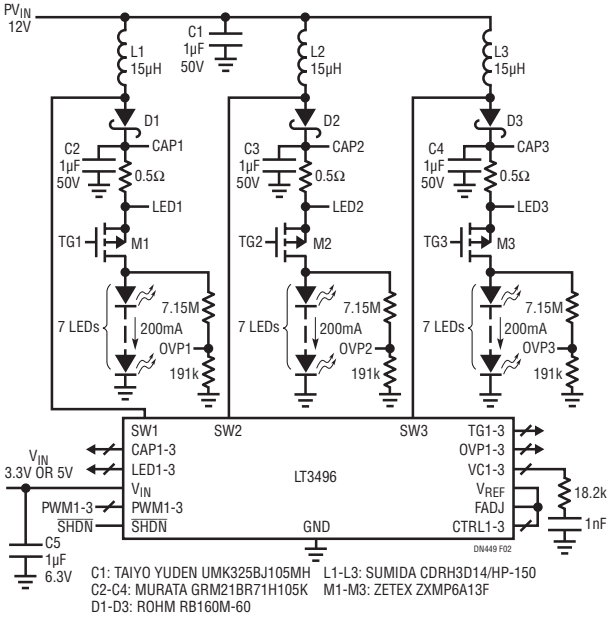
Integrated PMOS Drivers Improve PWM Dimming Ratio to 3000:1

A high PWM dimming ratio is critical in many display applications, especially in high end LCD panels. Beware, though, the definition of dimming ratio varies among suppliers. When comparing dimming ratios, pay close attention to the PWM dimming frequency and linearity of the LED average current at different PWM duty cycles. For instance, the LT3496's high 3000:1 PWM dimming ratio can be achieved at a 100Hz PWM frequency—high enough to keep the display flicker-free over the entire dimming range.



C1-C3, C7: MURATA GRM31MR71H105KA88 L1-L3: TAIYO YUDEN NP04SZB 100M
C4-C6: MURATA GRM188R71C474KA88 M1-M3: ZETEX ZXMP6A13F
D1-D3: DIODES DFLS160

Figure 1. Triple Buck Mode Can Drive 3x 500mA LED Strings



C1: TAIYO YUDEN UMK325BJ105MH L1-L3: SUMIDA CDRH3D14/HP-150
C2-C4: MURATA GRM21BR71H105K M1-M3: ZETEX ZXMP6A13F
D1-D3: ROHM RB160M-60

Figure 2. Triple Boost Mode Can Drive 200mA LEDs

Buck Mode Circuit Drives Three 500mA LED Strings

Figure 1 shows a triple buck mode LED driver. Each channel drives 500mA of current to its LEDs. Each string can have from eight to twelve LEDs, depending on type. The 2.1MHz switching frequency minimizes the solution size by allowing the use of low profile inductors and capacitors. The overall size of the circuit is less than 16mm × 16mm, with a maximum height of 1.5mm.

Efficiency can be above 95% for a LT3496 buck mode driver. A further reduction in the parts count is possible by removing M1, M2 and M3. However, the dimming ratio drops without those MOSFETs. To improve the efficiency, the V_{IN} pin should be biased from a 3.3V or 5V supply. Energy to the LEDs is supplied by PV_{IN}. OVP protection is omitted in Figure 1.

Boost Mode Circuit Drives Three 200mA LED Strings

Figure 2 shows a triple boost mode driver that delivers 200mA to each LED string from a regulated 12V. Figure 3 shows the superior PWM dimming performance of the circuit. The LED current reaches a programmed 200mA in less than 500ns. The efficiency of this circuit is 90% at a 2.1MHz switching frequency. Unlike the buck mode driver, the boost mode and buck-boost mode drivers always require an OVP circuit at the output for open LED protection.

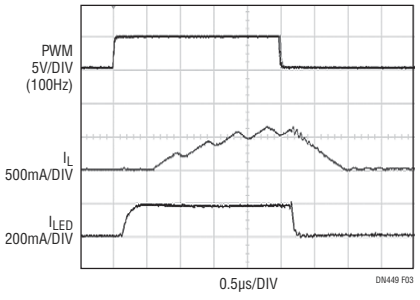


Figure 3. Achieving Greater Than 3000:1 PWM Dimming Ratio with a PMOS Disconnect

Buck-Boost Mode Circuit Survives Load Dump Events

In automotive applications, load dump is a condition under which an IC is expected to experience 40V transient. In such applications, the LED string voltage often falls in the middle of the 8V to 40V input supply range, thus requiring buck-boost mode.

In a buck-boost circuit, the switch voltage is the sum of the input voltage and the LED voltage. Therefore, it is necessary to turn off the internal power switch before the input voltage gets too high. The LT3496 circuit in Figure 4 drives four LEDs, at 200mA per channel. The circuit monitors the Schottky diodes' cathode voltage (V_{SC}). The OVP logic turns off the main switch when V_{SC} is above 38V, preventing the switch voltage from rising further. Since no IC pin experiences absolute maximum voltage, the circuit survives the load dump event.

Conclusion

Multiple output LED drivers, such as the LT3496, offer excellent current matching, efficiency and space savings. The flexibility to operate in buck, boost or buck-boost mode makes the LT3496 feasible in many rugged applications.

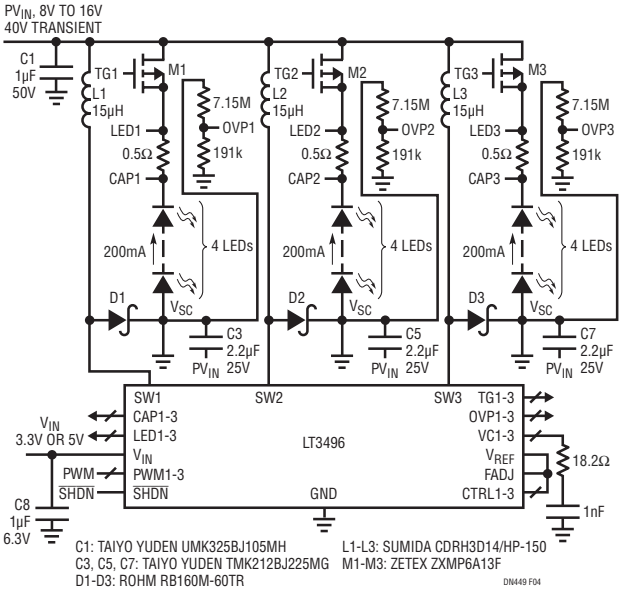


Figure 4. Triple Buck-Boost Mode Can Drive 200mA LEDs While Surviving Load Dump

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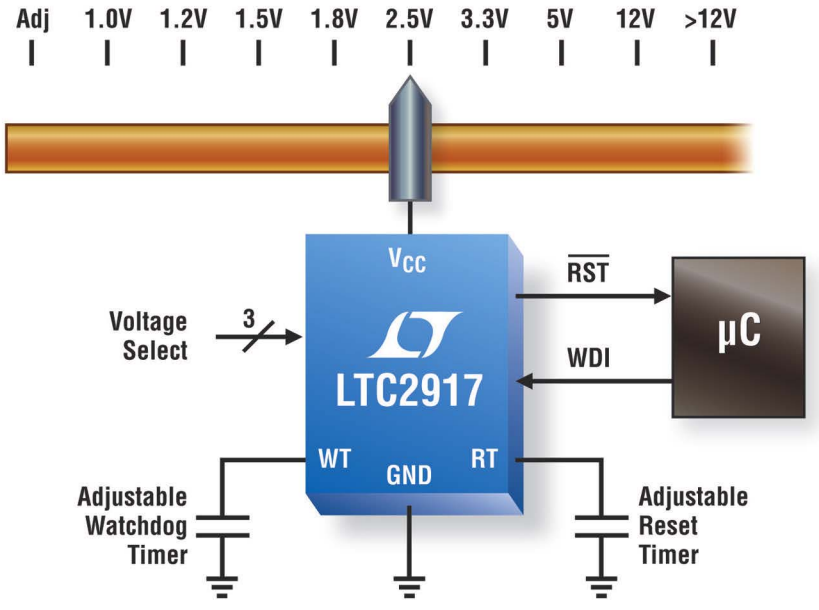

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LTC2916	1	Pin-Selectable	Pushbutton Input, 5% Tolerance, 9 Pin-Selectable Thresholds	TSOT23-8, 3 x 2 DFN-8
LTC2917	1	Pin-Selectable	Watchdog, 27 Pin-Selectable Thresholds, Pin-Selectable Tolerance: 5%, 10% or 15%	MSOP-10, 3 x 2 DFN-10
LTC2918	1	Pin-Selectable	Watchdog, Pushbutton Input, 5% Tolerance, 9 Pin-Selectable Thresholds	MSOP-10, 3 x 2 DFN-10
LTC2904/LTC2905	2	Pin-Selectable	27 Pin-Selectable Thresholds, Pin-Selectable Tolerance: 5%, 10% or 15%	TSOT23-8, 3 x 2 DFN-8
LTC2909	3	3 Resistors	Undervoltage/Overvoltage Monitor	TSOT23-8, 3 x 2 DFN-8
LTC2900/LTC2901/ LTC2902	4	2 Resistors	Watchdog, Individual Supply Comparator Outputs, Pin-Selectable Tolerance: 5%, 7.5%, 10% or 12.5%	MSOP-10, 3 x 3 DFN-10/ SSOP-16
LTC2908	6	2 Resistors	2 to 5 Adjustable Inputs, Tiny Package	TSOT23-8, 3 x 2 DFN-8
LTC2930/LTC2931 LTC2932	6	2 Resistors	Pushbutton Input, Watchdog, Individual Supply Comparator Outputs, Pin-Selectable Tolerance: 5%, 7.5%, 10% or 12.5%	3 x 3 DFN-12/TSSOP-20
LTC2910	8	2 Resistors	8 Adjustable Inputs	SSOP-16, 5 x 3 DFN-16

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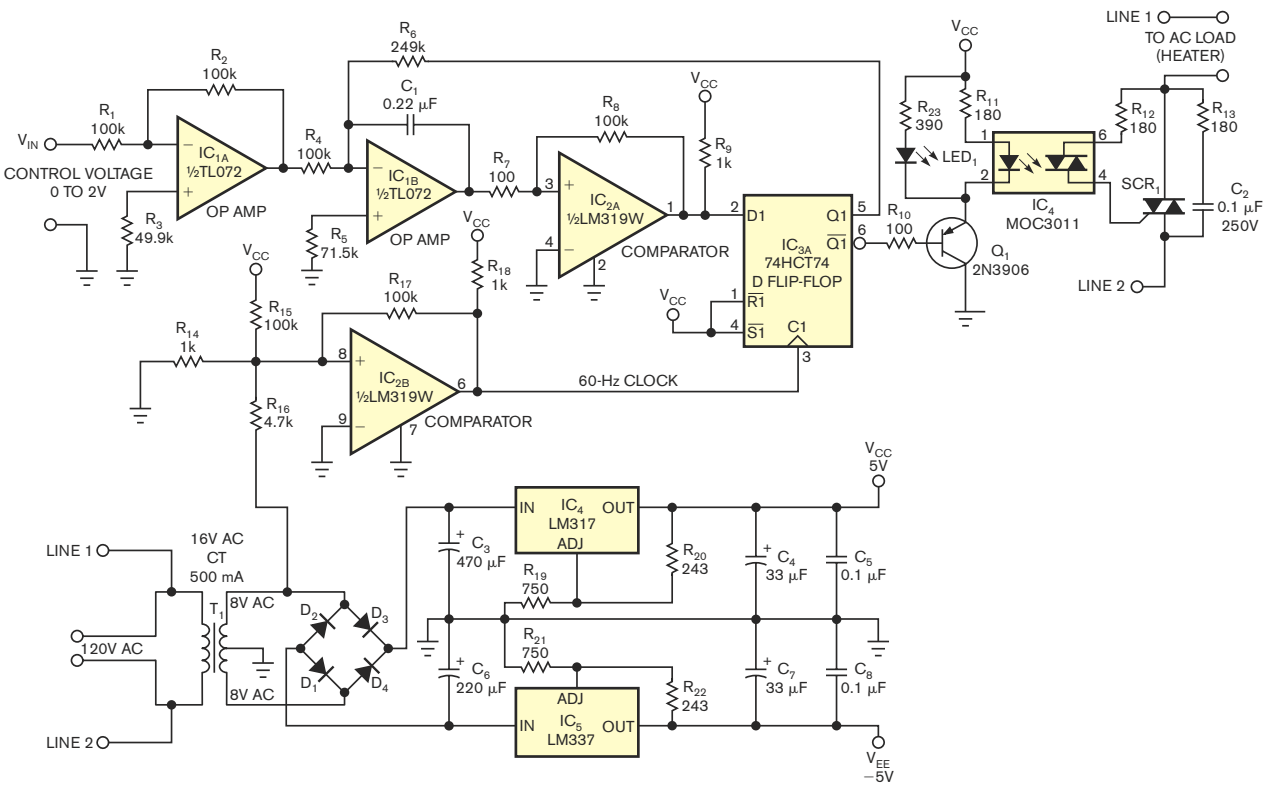

Figure 1 This ac controller borrows from a sigma-delta converter to output a number of whole cycles of ac-line power according to an input-control voltage.

voltage's input impedance is 100 kΩ.

The next stage, IC_{1B}, is an integrator. The integrator output ramps either up or down depending on the polarity of the input current. The speed at which it ramps depends on the magnitude of the input current. The integrator is the heart of the delta-sigma modulator. It forces a balance, on the average, between the control-voltage current in R_4 and the feedback current in R_6. In other words, the duty cycle of the output of IC_{3A}, a CMOS D-type flip-flop, must match the control-voltage percentage of full-scale.

Comparator IC_{2A} detects whether the integrator's output is positive, thus requiring more feedback current, or negative, thus requiring less feedback to maintain the balance. The output of the comparator switches between 0 and 5V. The flip-flop latches the comparator's decision on the next rising edge of the 60-Hz clock.

PNP transistor Q_1 and optoisolated SCR (silicon-controlled rectifier) IC_4 drive load-switching SCR_1 into conduction whenever the flip-flop provides feedback current to the integrator. Indicator LED_1 lights when the load SCR is on. The secondary of transformer T_1 detects the zero crossings of the ac-power line; these crossings provide the 60-Hz clock. The output of comparator IC_{2B} switches high during the positive half-cycles of the ac line and low during the negative half-cycles. Resistor R_{15} provides a small positive bias, causing the edges of the 60-Hz clock to occur slightly early—which is better than late in this case. If you turn off the SCR too late, its self-latching nature may cause it to stay on for an extra half-cycle when it should have been off.

IF YOU TURN OFF THE SCR TOO LATE, ITS SELF-LATCHING NATURE MAY CAUSE IT TO STAY ON FOR AN EXTRA HALF-CYCLE WHEN IT SHOULD HAVE BEEN OFF.

Both comparators IC_{2A} and IC_{2B} use a small amount of hysteresis to promote fast, clean switching. The remaining components generate the regulated 5 and −5V power supplies. Transformer T_1 and optoisolator IC_4 provide isolation from the ac-power line.

This Design Idea works well for an application such as a spa-heater control but does not work for light-dimming or motor-speed control because the output power is pulsating in nature. You can easily adapt the design for 240V-ac or 50-Hz operation. EDN

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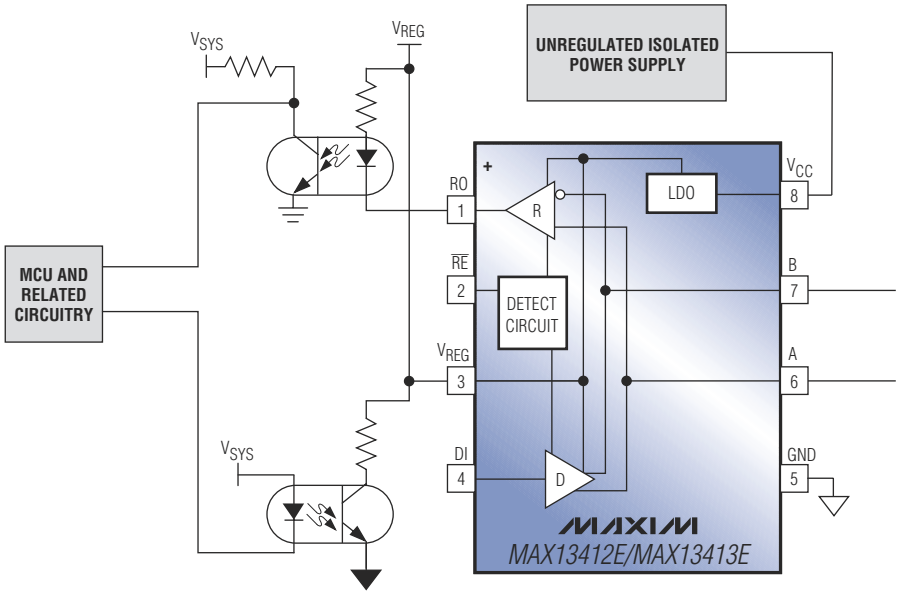

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Extend monolithic programmable-resistor-adjustment range with active negative resistance

W Stephen Woodward, Chapel Hill, NC

A variety of solid-state, in-circuit-programmable replacements exist for the traditional electromechanical trimmer potentiometer. These replacements have many obvious advantages, such as automatic adjustability, miniaturization, and immunity to vibration. But these devices, unlike humble mechanical potentiometers, have relatively large minimum programmable resistance. Although you can adjust a typical trimming potentiometer down to a fraction of 1Ω, solid-state-potentiometer substitutes usually bottom out at 10s, 100s, or even 1000s of ohms. This limitation can sometimes be problematic and frequently precludes use of the solid-state option in some design applications.

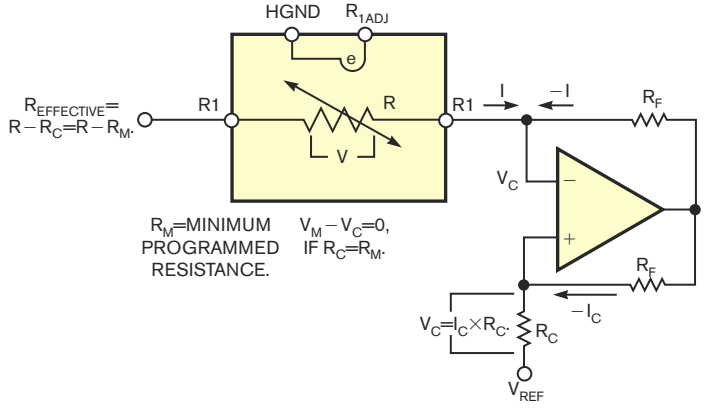

Figure 1 This circuit uses an op amp in a negative-resistance topology that, in effect, subtracts the minimum programmable resistance from the total programmed resistance.

The Rejustor family of devices, which Microbridge (www.mbridgetech.com) recently introduced, provides an extreme example of this effect. You can program a typical Rejustor over only a narrow span of 30%. For example, you can program a 10-kΩ Rejustor to no lower than 7 kΩ, imposing a serious and obvious obstacle to general-purpose application of these devices. **Figure 1** suggests a generally applicable workaround that works not only with Rejustors, but also with all adjustable resistances. It uses an op amp in a negative-resistance topology that, in effect, subtracts R_{MIN} (minimum programmable resistance) from the total programmed resistance. EDN

1-Wire network controls remote SPI peripherals

Michael Petersen, Maxim Integrated Products, Colorado Springs, CO

Many 1-Wire-compatible peripherals are available, but, for those that lack the 1-Wire capability, the circuit in **Figure 1**, pg 80, illustrates one way to implement it. The example controls a remote LED display by the 1-Wire network through an SPI (serial-peripheral-interface)-compatible display controller.

To produce the three-wire SPI that a MAX7221 display controller requires for the $\overline{CS}$ (chip-select), DIN (serial-data), and CLK (clock) signals, the 1-Wire network serially addresses three DS2405 1-Wire switches. The first switch directly creates $\overline{CS}$; the second switch directly creates DIN; and the third switch, aided by three exclusive-OR gates, creates CLK.

The edge detector and one-shot IC_{4A}, IC_{4B}, and IC_{4C} combine the outputs of IC_2 and IC_3—Data 1 and Data 0—to create a clock signal for the SPI. This one-shot clock-generation circuit improves the data rate by requiring only a single 1-Wire transaction per SPI bit, instead of the three transactions—data, clock low, and clock high—that would be necessary if you directly use the IC_3 output as a clock signal.

To transmit data to the SPI inputs, first set the output of IC_1 low. Then, transmit the data bits using the following rules: If the current data bit differs from the previous bit, set IC_2's Data 1 output accordingly. If the current data bit is the same as the previous bit, toggle IC_3's Data 0 output. The circuit automatically generates a clock pulse each time and requires only one 1-Wire command for each data bit sent. When data transmission is complete, send a final 1-Wire command to set the IC_1 output high.

This circuit allows a 1-Wire network to control a remote temperature display, but similar techniques can provide an interface to I^2C (inter-integrated-circuit)-compatible devices and to other SPI peripherals, such as ADCs and DACs. You can also produce a bidirectional-data capability by adding a fourth DS2405. Note that the SPI data rate and updates to the peripheral are relatively slow, but speed is not an issue for many remote-monitoring applications. EDN

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Part	Description	Interface	Authentication Feature
DS28CN01**	1kb EEPROM with SHA-1	I²C/SMBus™	Bidirectional SHA-1 challenge and response
DS28E01-100**	1kb EEPROM with SHA-1	1-Wire®	Bidirectional SHA-1 challenge and response
DS2401/DS2411	64-bit ROM serial number	1-Wire	Customized 64-bit ROM
DS28CM00	64-bit ROM serial number	I²C/SMBus	Customized 64-bit ROM
DS2431	1kb EEPROM	1-Wire	Customized 64-bit ROM, WP/OTP modes
DS2460**	SHA-1 coprocessor	I²C	Secure storage of system secrets

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1-Wire is a registered trademark of Maxim Integrated Products, Inc.
*Authentication solutions starting as low as $0.15 for consumer-electronics volumes. Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates. Not all packages are offered in 1k increments, and some may require minimum order quantities.
**Data sheet provided under NDA.

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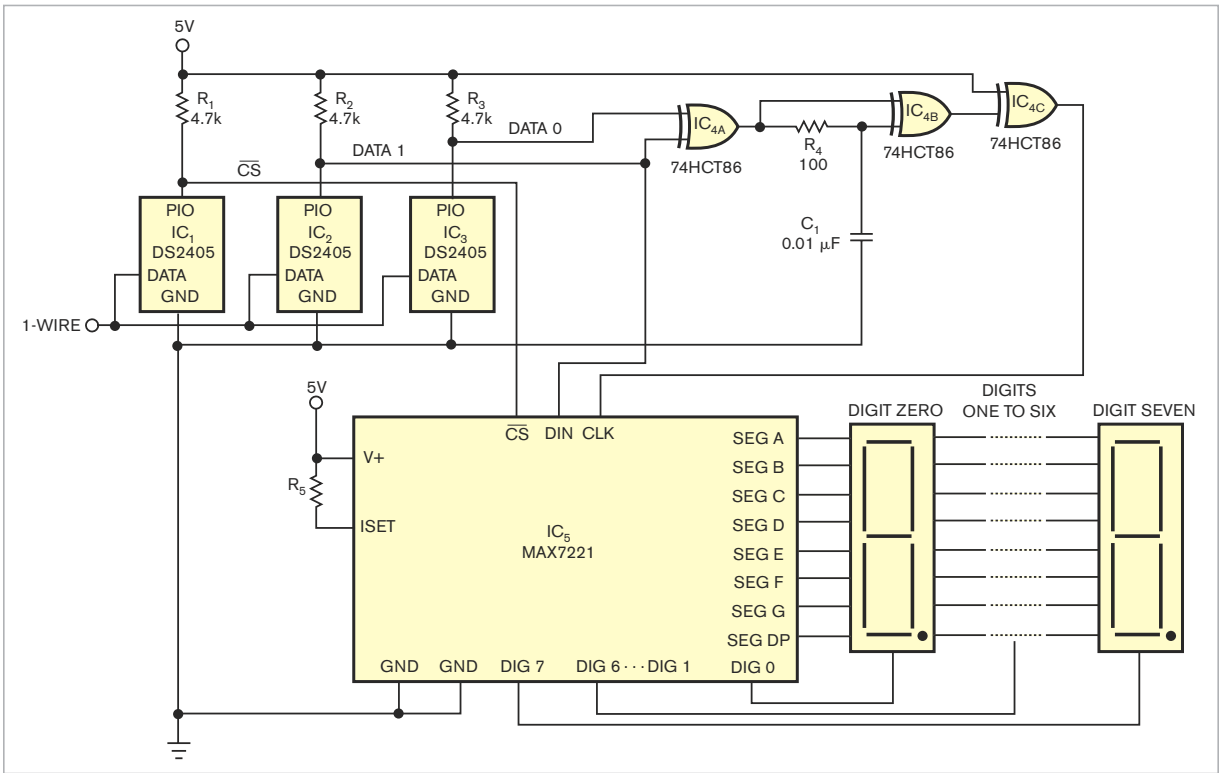
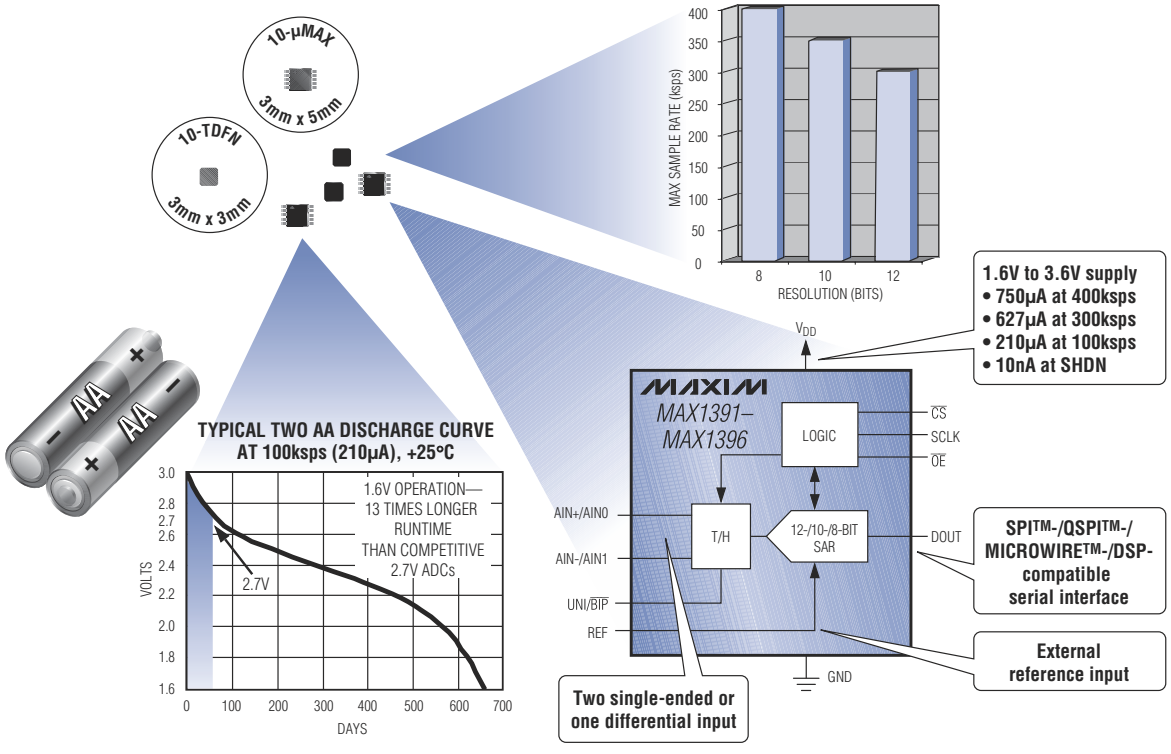


Figure 1 Three 1-Wire switches–IC_1, IC_2, IC_3; three XOR gates, IC_4; and the associated components enable a 1-Wire network to control this display through the SPI peripheral IC_5.

Ultra-low-power 12-/10-/8-bit ADCs run on two AA batteries* for 1.8 years at 100ksps



- 1.6V to 3.6V low-power operation
- 0 to V_{DD} external reference input
- Unipolar or bipolar operation
- One differential or two single-ended inputs

Part	Resolution (Bits)	No. of Channels	Speed (ksps)	INL (LSB)	DNL (LSB)	SINAD (dB)	Package	Price† ($)
MAX1391/94	8	1 diff/2 SE	400	±1	±1	49	10-TDFN/µMAX®	1.15
MAX1392/95	10		350			61		1.81
MAX1393/96	12		300			70		2.48

*3300mAh AA alkaline battery (LR6).
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µMAX is a registered trademark of Maxim Integrated Products, Inc.
†1000-up recommended resale. Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates. Not all packages are offered in 1k increments, and some may require minimum order quantities.

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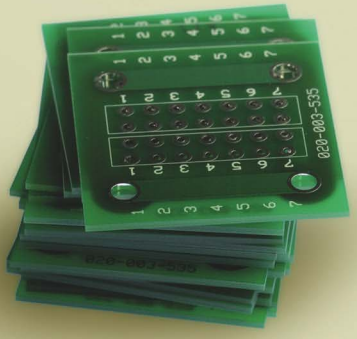

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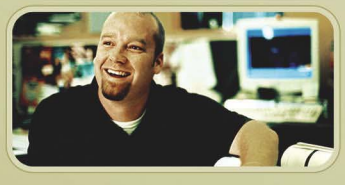

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POWER SOURCES

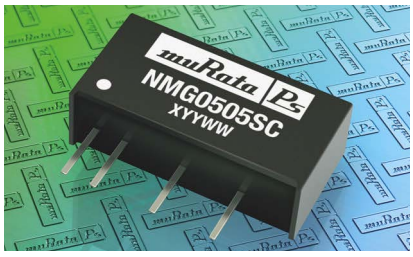
Switcher ICs allow for compact notebook-adapter designs

With an ultralow-profile package, the TOPSwitch-HX IC power-package family suits use in 65W adapters for notebook computers and 20 to 100W power supplies for LCD monitors and flat-panel TVs. The switcher ICs meet Energy Star 2.0 specifications for external adapters and target reference designs, such as the DER-196, for a 65W notebook adapter measuring slightly larger than a standard deck of playing cards. An L-shaped lead bend allows the vendor's eSIP package to lie flat against the PCB with the heat-sink pad facing up. Combining a 700V switching-power MOSFET with controller and supervisory functions, the 2-mm-high IC also provides space for a heat sink. Available in eSIP-L packages, the TIP260LN, the TOP261LN, and the TOP262LN IC power packages suit 20 to 100W power levels and cost $1 (10,000).

Power Integrations, www.powerint.com

2W dc/dc converters feature a variety of input and output voltages

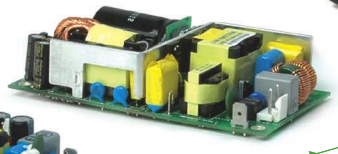
Aiming at isolating and converting dc-power rails, the isolated, 2W NMG single-output-dc/dc-converter series has a pin-compatible power-upgrade path from the vendor's 1W NMR series. Galvanic isolation allows you to configure the devices to provide an isolated negative rail in systems having only positive rails. Requiring no external heat sink, the converter operates over a −40 to +85°C temperature range. The series provides either 5 or 12V input voltages; 5, 9, 12, or 15V output voltages; a claimed 88% efficiency; and 1-kV-dc isolation voltages. Available in 19.5×7.5×10-mm SIP packages, the NMG series costs $8 (1000).



Murata Power Solutions, www.murata-ps.com

EFFICIENT POWER

While the world around you goes green, CUI and V-Infinity can keep you one step ahead of the efficiency curve. CUI offers a large selection of EISA 2007, CEC Level IV, and Energy Star compliant external power supplies with RoHS compliance and UL approvals. Efficient internal power supplies from V-Infinity include compact switching regulators and open frame switching power supplies.



V78 series

- dc switching regulator
- pin compatible with 78XX linear regulators
- 500 and 1000 mA output current models
- efficiency up to 96%
- no need for a heatsink
- wide input range
- thermal shutdown
- low ripple and noise
- non-isolated
- short circuit protection

USB style series

- switching power supply
- 2.5 & 5 W output power
- USB type A receptacle output
- Energy Star / CEC / EISA 2007 compliant
- insulation resistance 100 M Ohm at 500 V dc
- no-load power consumption 0.5 W max.
- universal input
- UL/cUL approvals
- RoHS compliant

EMT series

- switching power supply
- 30 W output power
- interchangeable blades
- ac power cord inlet
- Energy Star / CEC / EISA 2007 compliant
- insulation resistance 50 M Ohm at 500 V dc
- no-load power consumption 0.5 W max.
- universal input
- UL/cUL, CE, FCC; TUV/GS, C-Tick approvals
- RoHS compliant

VMS-160 & VMS-365 series

- switching power supply
- **VMS-160**: 160 W output power in a 2”x 4” footprint and 18.2 W/in³ power density
- **VMS-365**: 365 W output power in a 3”x 5” footprint and 19 W/in³ power density
- single output voltages of 5, 12, 24, and 48 V dc
- 90% typical efficiency
- medical approvals
- universal input (90 – 264 V ac)
- built-in active PFC function
- 12 V auxiliary fan output

AC-AC series

- linear power supply
- 3 – 12 W output power
- 6ft. cord length - custom lengths available
- output voltage tolerance: ±5 % at rated load
- class 2 power supply
- Energy Star / CEC / EISA 2007 compliant
- no-load power consumption 0.5 W max.
- North American wall plug
- UL/cUL approvals
- RoHS compliant

CEC Level IV- The California Energy Commission has mandated requirements for power supplies used with certain types of products. The most current requirements are the same as the EISA 2007 requirements and are referred to as either “Tier 2” or “Level IV.”

Energy Star- Energy Star is a joint program of the US Environmental Protection Agency (EPA) and the US Department of Energy (DOE) aimed at preserving the environment through energy efficiency. Adapters meeting the Energy Star guidelines are up to 30% more efficient than non-compliant versions and must meet both active and no-load minimum efficiency requirements set forth by the EPA and DOE. Compliance with these requirements is voluntary.

EISA 2007- The Energy Independence and Security Act of 2007 was passed by Congress in December of 2007 and addresses minimum efficiency standards for external power supplies manufactured on July 1, 2008 and after. This law stipulates the energy efficiency criteria for adapters in active mode depending upon their power rating. The stipulated energy consumption for all adapters in no-load mode must be less than 0.5 W according to EISA 2007. Compliance with these requirements is mandatory.

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POWER SOURCES

Dual-output converters meet military standard 704B-F

The MTC15 and MTC30 dual-output converters join the vendor's MTC series of fully encapsulated COTS (commercial-off-the-shelf), 4 to 35W dc/dc converters. Providing a ±12 or a ±15V-dc output and a 15.5 to 40V-dc input range, the converters target military and avionic platforms requiring a 28V-dc input. The converters suit 10V transients for 10 sec and 50V dc for 1 sec, meeting military standard 704B-F. They can draw as much as 80% of the output power from the positive or the negative output, as long as they do not exceed the maximum output power. A feedback loop constantly monitors the outputs in order, providing a high degree of load regulation. The 15W MTC15 dual-output unit costs $203.

XP Power, www.xppower.com

Dual low-dropout regulators claim high conversion efficiency

The low-input-voltage-capable MIC5313/4/5/6 family integrates two low-dropout regulators operating from a 1.7V input voltage at a 37-µA total quiescent-current consumption. To regulate low-voltage rails and provide improved conversion efficiency, the family's design allows very low-dropout voltages. The dual regulators supply as much as 300-mA output currents and consume 37-µA quiescent current with both channels on. The device's low quiescent voltage, low input voltage, and low quiescent current make it suitable in applications requiring continuous power-up. The family allows the use of small ceramic output capacitors to reduce required board space. The MIC5313 and 15 come in 2×2-mm MLF-10 lead packages, and the MIC5314 and 16 come in 2.5×2.5-mm MLF-12 lead packages. Operating over a −40 to +125°C temperature range, the MIC5313/4/5/6 cost $1.29 (1000) each.

Micrel, www.micrel.com

PC-power-supply device meets 80 Plus Gold standard

With 90% efficiency, the GreenChip PC chip set meets the Ecos Consulting and 80 Plus Program requirements for certification for a reference design. The PC-power-supply reference device features a secondary-side-controlled-switch concept and an active-clamp reset with an integrated switch, lowering the breakdown-voltage demand for the power components. The chip set fits standard ATX-size boxes. Comprising the TEA1771, the TEA1781, and the TEA1782 chips, the GreenChip PC chip set sells for $4 to $5.

NXP Semiconductors, www.nxp.com

DC/DC-converter series provides as much as 165W output-voltage tracking

Adding eight dc/dc converters to the Senpai series, the FPMS12T and the FPLS12T nonisolated point-of-load converters operate over a 6 to 14V-dc input bus with a 0.75 to 5.5V-dc programmable-output voltage. The converters incorporate an output-voltage-tracking function, enabling various sequenced-power-up and power-down scenarios when using multiple converters. The FPMS12T devices deliver 55W of output power at a 600W/in.^{3} power den-

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productroundup

POWER SOURCES

sity, and the FPLS12T converters deliver 165W of output power at a 560W/in.^{3} power density. The devices feature little or no derating up to 85°C. An output-voltage-tracking function supports sequential, simultaneous, and ratiometric sequenced-start-up and -shutdown scenarios. Available in a 25.4×12×4.95-mm SIP package, the FPMS12T offers 6, 8, and 10A output-current models; the FPLS12T comes in a 50.8×13.6×7-mm SIP package in 10, 16, 20, 25, and 30A output-current models. Prices for the FPMS12T converters start at $7; prices for the FPLS12T series start at $11.
FDK Corp, www.fdk.com

INTEGRATED CIRCUITS

SOC supports range of options for fax machines

Targeting use in fax machines with ink-jet-, laser-, or thermal-printing capabilities, the SX9543X SOC provides direct printer control and USB interfaces. Features include dual-voice ADCs and DACs; multiple voice inputs and outputs, including a speaker amplifier; a cross-point switch; and additional ADCs for scanner and other analog-sensor inputs. Powered by a 180-MHz, 32-bit RISC processor, the device includes a 120-MHz, DSP-based image processor and three 288-MHz, flexible-I/O processors. The I/O processors enable connections to a variety of peripherals, such as scanners, printers, memory cards, and LCDs. The SOC comes in an exposed-pad QFP-176, and prices range from $7 to $15.
Conexant Systems, www.conexant.com

500-mA buck regulator provides an integrated dual-power monitor

Suiting 24V utility-metering, sensor-interfacing, and other industrial-motion-control and battery-powered-data-acquisition equipment, the AS7620 hysteretic 32V step-down regulator provides early-power-fail warning and power-good signals to microcontrollers. The 500-mA buck regulator provides an integrated dual-power monitor, a fixed 3.3V output, or an adjustable output voltage of 1.2V to the input voltage. The regulator provides soft-start, current limiting, and thermal shutdown, drawing a 1-mA current during shutdown. Claiming 93% efficiency, the device integrates a 100% duty cycle, extending operation in low-dropout conditions. A pin-selectable peak-current limit reduces component size by adjusting inductor selection. Operating over a −40 to +85°C industrial-temperature range, the regulator also provides 37-µA operation when delivering 500-µA output current. Available in a 4×4-mm MLPQ-12 package, the AS7620 dc/dc converter costs $1.36.
austriamicrosystems, www.austriamicrosystems.com

Digital-media processor integrates video-processing subsystem

Powered by an ARM926EJ-S core operating as fast as 270 MHz, the DM335 digital-media processor integrates a video-processing subsystem, enabling a 720p, high-definition video display in portable-system applications. Measuring 13×13×0.64 mm, the processor comes in a BGA-329 package. The TMS320DM335 digital-media processor costs $10.48. The TMDSEVM355 digital-video-evaluation module costs $495.
Texas Instruments, www.ti.com

productroundup

INTEGRATED CIRCUITS

Logic-gate optocouplers have high bandwidth

Aiming at Profibus, DeviceNet, CAN, and RS-485 industrial-communication standards, the FOD0710, FOD0720, and FOD0721 high-speed logic-gate optocouplers meet the qualifications for the UL1577 standard. The 25-Mbps-bandwidth devices feature 13-mA supply currents, 4.5 to 5.5V supply voltages, and 20-kV/µsec minimum common-mode-noise-rejection ratings. The vendor claims that the devices' lead-free, coplanar packaging reduces package capacitance by more than 30%. The FOD0710, FOD0720, and FOD0721 optocouplers cost $2.21, $2.44, and $2.67 (1000), respectively.

Fairchild Semiconductor, www.fairchildsemi.com

COMPUTERS AND PERIPHERALS

Tiny, 8-Gbyte storage device has gold plating

The 8-Gbyte STU8GPCG 24-carat-gold-plated storage device weighs less than 4.7g. Measuring 31.3×12.4×3.4 mm, the device comes in a gold-plated steel case. Available from www.newbiiz.com or www.newegg.com, the STU8GPCG storage device costs $40.

Super Talent Technology, www.supertalent.com

LCD monitor connects to HDMI

The MultiSync EA (enterprise-advanced) series includes the 26-in. EA261WM desktop-LCD monitor. Features include a WUXGA (wide-ultra-extended-graphics array), 1920×1200-pixel resolution, 400-cd/m^2 brightness, a 1000-to-1 contrast ratio, a four-port USB hub, and a 5-msec response time. Using an adapter, the device is HDMI-capable, providing 720p and 1080p from DVI-D (digital-visual-interface digital). Using HDCP, the display provides a 92% color gamut. The EA261WM desktop-LCD monitor costs $679.99.

NEC Display Solutions, www.necdisplay.com

Graphics cards provide as much as 1024 Mbytes of frame-buffer memory

The XLR8 GeForce 200 series includes the GTX 260 PCIe 2 and the GTX 280 PCIe 2 graphics cards. The GTX 260 features 896 Mbytes of GDDR3 frame-buffer memory, a 576-MHz core clock, and a 1242-shader clock. The card has a 111.9-Gbps memory bandwidth, 36.9 billion/sec texture-fill rate, and 2000-MHz effective data rate. The GTX 280 provides 1024 Mbytes of GDDR3 frame-buffer memory, a 602-MHz core clock, and a 1296-shader clock. The 280 has a 141.7-Gbps memory bandwidth, 48.2 billion/sec texture-fill rate, and 2214-MHz effective data rate. The GTX 260 PCIe 2 and the GTX 280 PCIe 2 graphics cards cost $649.99 and $399.99, respectively.

PNY Technologies, www.pny.com

Discrete device combines handset-audio filtering and ESD protection

Combining handset-audio filtering and ESD protection, the EMIF06-

COMPUTERS AND PERIPHERALS

AUD01F2 device suits portable consumer headsets, including mobile phones and MP3 players. The vendor claims a 77% reduction in board space, compared with previous discrete products. Available in a 2.42×1.92-mm flip-chip package, the EMIF06-AUD01F2 costs 55 cents (1000).
STMicroelectronics, www.st.com

Stream processor breaks 1-Tflop barrier

Occupying a single PCI slot, the FireStream 9250 Stream processor breaks the 1-Tflop barrier. The device has 150W power consumption, with as many as 8 Gflops/W. A double-precision, floating-point hardware implementation delivers more than 200 Gflops. The FireStream 9250 and the supporting software-development kit cost $999.
Advanced Micro Devices, www.amd.com

Mac memory kit suits Mac Pro desktops

The fully buffered Mac memory kit comes in a 4-Gbyte, 2×2-Gbyte module. The 800-MHz memory kit targets recent Mac Pro desktop systems. The 4-Gbyte Mac memory kit costs $250.
Corsair, www.corsair.com

EDN ADVERTISER INDEX

Company	Page
Actel Corp	6
Advanced Interconnections	38
Agilent Technologies	17
Altera Corp	61
Analog Devices Inc	21
	23
	C-3
Ansoft Corp	58
austriamicrosystems AG	80
Bourns Inc	3
BuyerZone	86
Central Semiconductor Corp	32
Cirrus Logic Inc	2
Coilcraft	11
CUI Inc	84
Cypress Semiconductor	C-4
Digi-Key Corp	1
Digi International-Rabbit	52
EMA Design Automation	47
Express PCB	56
GaGe	68
ICS Electronics	46
International Rectifier Corp	9
Intersil	33, 35
	36, 37
Keil Software	88
Lattice Semiconductor	34
LeCroy Corp	C-2
Linear Technology Corp	70, 75
	73, 74
MathWorks Inc	27

Company	Page
Maxim Integrated Products	77
	79, 81
Melexis Inc	19
Memory Protection Devices	66
Mentor Graphics	83
	85, 87
Messe Muenchen GmbH	63, 65
Micrel Semiconductor	12
Microchip Technology	43
Mill Max Manufacturing Corp	55
Monolithic Power Systems	53, 64
Mouser Electronics	8
National Instruments	4, 13
NewarkInOne	25
Noritake Co Inc Electronics Division	28
Pico Electronics	39
	50, 54
Radicom Research	89
Stanford Research Systems Inc	62
Summit Microelectronics	48
Sunstone Circuits Inc	82
Tektronix	31
Tern	89
That Corp	56
Toshiba America	14
	45, 57
Vicor Corp	51, 67
Xilinx Inc	69

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The case of the stolen capacitor

DANIEL VASCONCELLOS

It was the usual team project: a group leader with overall responsibility for the end product, with assistant designers working on specialized subsystems. I was designing the fiber-optic-communications links for the product, and, not wanting the noisy 5V digital-V_{CC} supply to contaminate my sensitive analog circuits, I elected to linearly regulate the 12V down to a reasonably clean 5V to keep my analog circuits happy. The data sheet instructed me to include 10 µF of stabilizing capacitance at the input to my voltage regulator. Read on to learn the very good reason for this inclusion.

In the week before shipping the product, a horrendous problem emerged. Hot-plugging a card into the live backplane caused a glitch on the system's 5V rail and caused the main processor card to restart. Oops! I managed to arrive at a Band-Aid solution to that problem by attaching tantalum capacitors and fuses across the 5V rail on the backplane at every card slot. I then suggested that we should perhaps also look at the hot-plug effect on the 12V rail.

Surely enough, a similar problem resulted; hot-plugging caused a glitch on the 12V rail, in turn causing another colleague's PLL (phase-locked loop) to hiccup. This glitch did not bother my 12 to 5V regulator because it had lots of filtering on the output side.

So, the team lead came up with a "fix" that resulted in the insertion of a resistor that effectively separated the capacitor from my regulator and stole my regulator's input capacitor for use in the PLL-filtering function. When I saw his ECO (engineering-change order), I told this colleague that this fix was not doable: I needed that capacitor for my regulator. His reply was that our prototypes worked without the capacitor on my regulator and that it was too labor-intensive to attach another capacitor during the assembly rework. (Another "Oops!" ensued.) I did not press the point; after all, it was his circuit card, and, as group leader, he made the final decisions.

Six months went by with no problems. Then reports suddenly started coming in from the field that new-production cards would not work when customers installed them into systems. The clincher occurred when a field engineer called us to ask whether it was normal to have a 10-MHz sine wave riding on the 12V rail. We investigated, and found that the production department had changed to a new vendor of the voltage regulators. The new units were some no-name brand for a few pennies less and with no vendor logos or markings on the parts. What's worse, the production department did not keep the necessary records to indicate the original manufacturer. Nevertheless, these regulators really *did* require some input stabilizing capacitance.

The result was the addition of capacitors that we should have included during the initial rework, even though it was too labor-intensive. Yet, it would have been far less-labor intensive than the resulting recall of the cards.

I learned a good lesson from that experience. Even though it was ultimately not my responsibility, I should have insisted that the team leader include the additional capacitor. I have since applied this lesson to later team-design issues, and some people now think of me as an ornery old curmudgeon, but the resulting designs always worked properly. EDN

You can reach design consultant Glen Chenier at glen@teetertottertreestuff.com. Like him, you can share your Tales from the Cube and receive $200. Contact edn.editor@reedbusiness.com.

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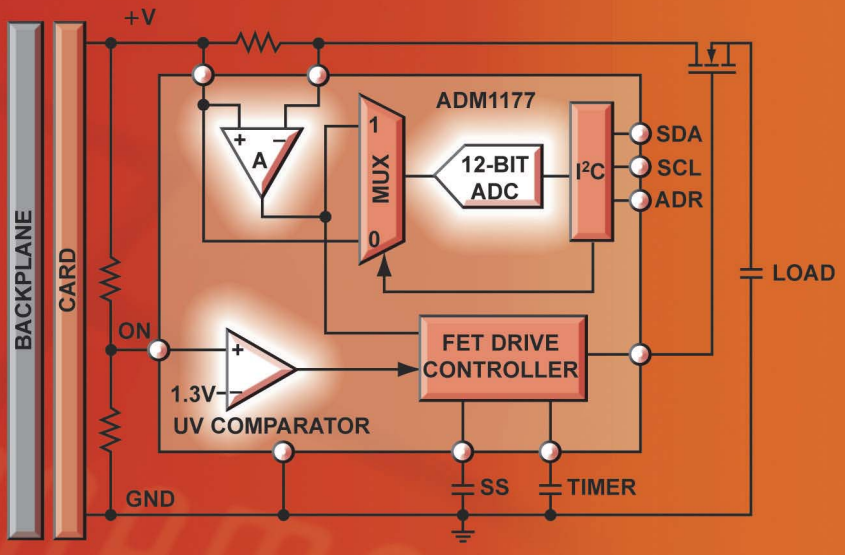
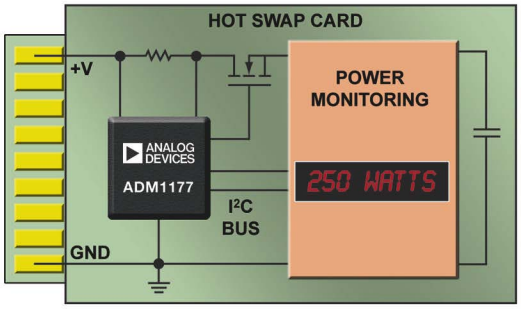
Look what 40 years of analog leadership does for power management ICs.



Hot Swap controllers with integrated power monitors

Integrated 12-bit ADC and accurate current sense amplifier deliver the industry's most accurate and smallest solution.

Hot Swap ICs with precision ADC deliver greater accuracy for improved energy savings.



Industry's most accurate Hot Swap and power monitor ICs provide accurate data on power consumption, enabling better control and conservation of energy.

Let us show you how we're applying more than four decades of analog expertise to power management and delivering industry-best solutions that differentiate your designs and add value for your customers. Case in point: we've integrated industry-leading converter and amplifier cores with Hot Swap controllers to provide unmatched ±3% power monitoring accuracy, allowing you to offer your customers increased energy savings opportunities for data center applications.

Put our analog leadership to work with your power designs. Contact ADI's power technical support at *power.management@analog.com*.

Part Number	Hot Swap Range (V)	Integrated Power Monitoring	Features	Package	Price @ 1k ($U.S.)
ADM1175	3.15 to 16.5	Yes	Manual convert pin	10-lead MSOP	2.50
ADM1176	3.15 to 16.5	Yes	16 I²C addresses	10-lead MSOP	2.50
ADM1177	3.15 to 16.5	Yes	Dedicated SOFT START pin	10-lead MSOP	2.50
ADM1178	3.15 to 16.5	Yes	Overcurrent ALERT pin	10-lead MSOP	2.70
ADM1170	1.6 to 16.5	No	Separate VCC pin	8-lead TSOT	2.10
ADM1171	2.7 to 16.5	No	Current sense output	8-lead TSOT	2.20
ADM1172	2.7 to 16.5	No	Power fail comparator	8-lead TSOT	2.00

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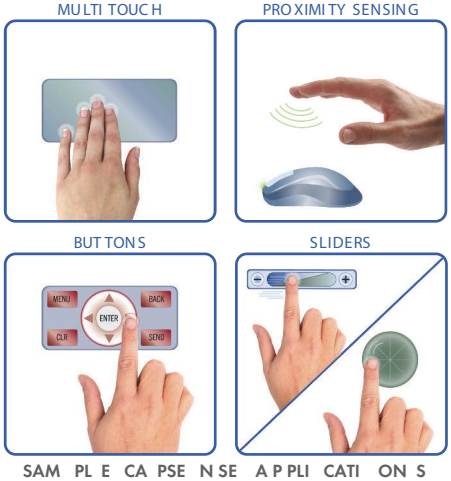

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